BIST in the Sync Tx/Rx

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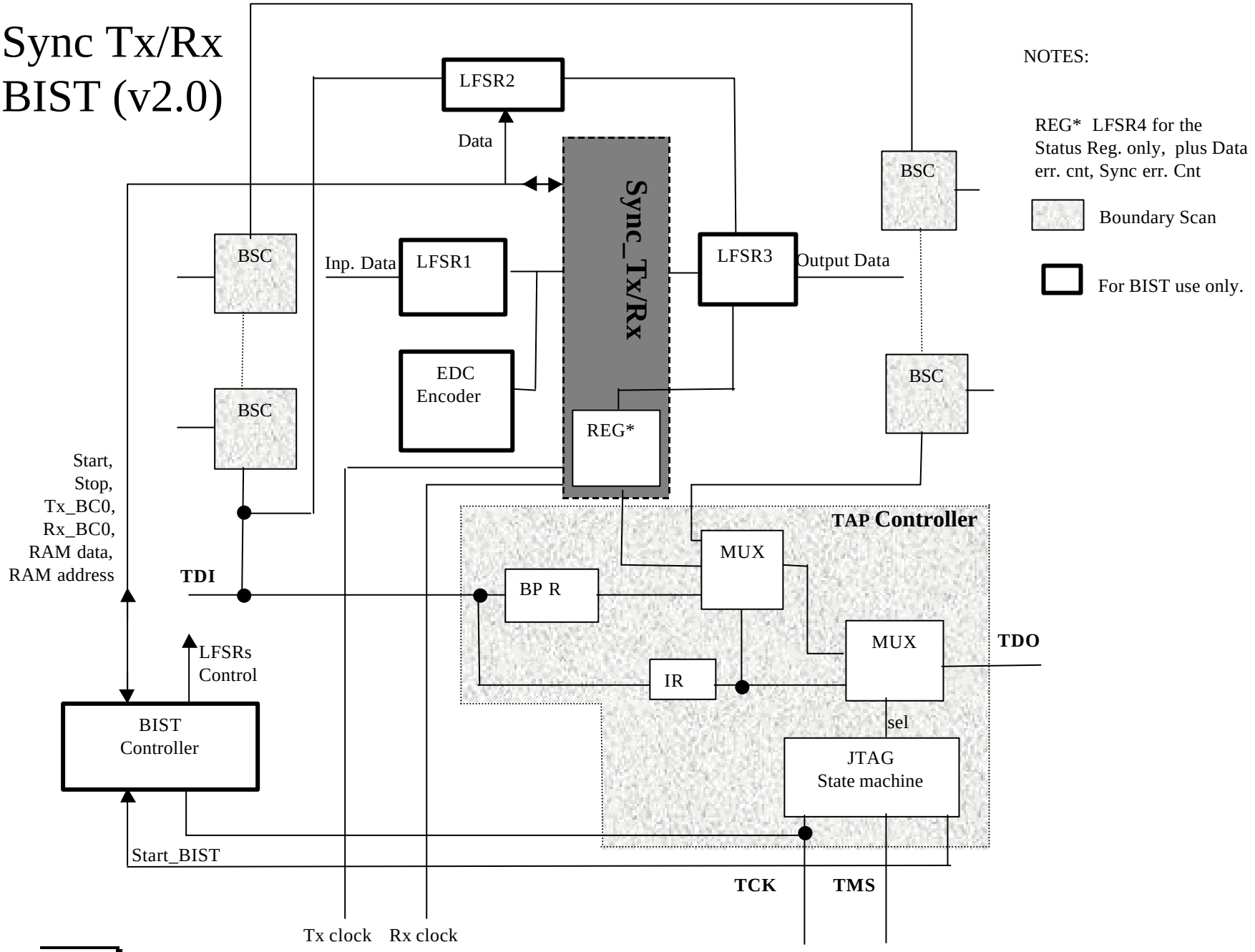
Portugal / CMS Meeting

November 2000, LIP, Lisbon

Outline

- Overview of the BIST architecture
- BIST solutions for ALTERA ACEX1K
  - ALTERA and IEEE 1149.1
  - Signature Shift
  - Start BIST Command
- BIST Quality Evaluation
- Conclusions

Sync Tx/Rx BIST (v2.0)



NOTES:

REG* LFSR4 for the Status Reg. only, plus Data err. cnt, Sync err. Cnt

Boundary Scan

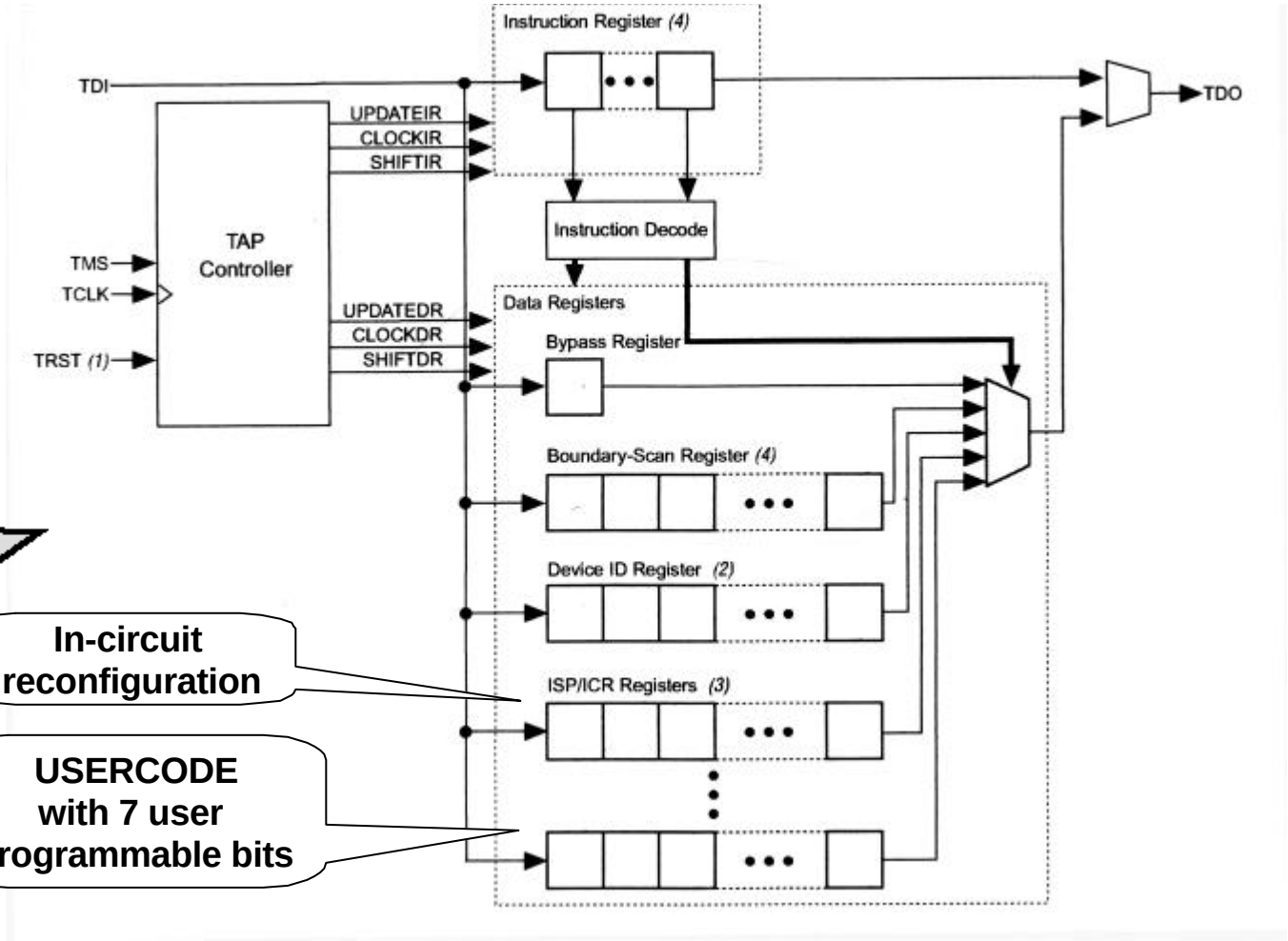
For BIST use only.

BIST solutions for ALTERA

ALTERA

and

IEEE 1149.1



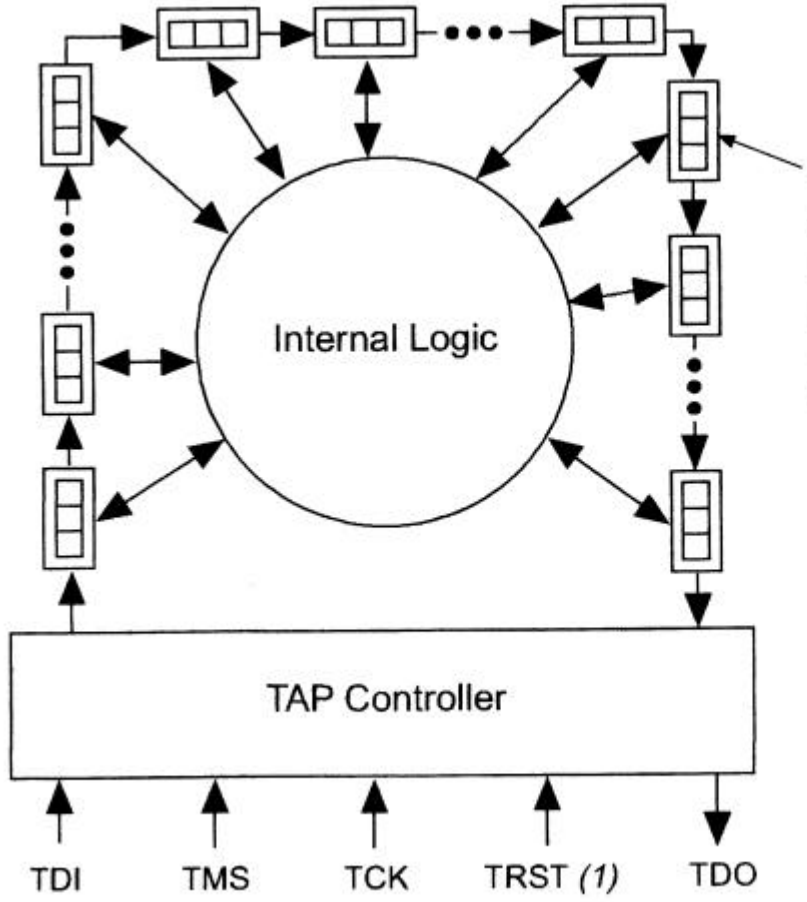
No support for user definable registers

In-circuit reconfiguration

USERCODE with 7 user programmable bits

BIST solutions for ALTERA

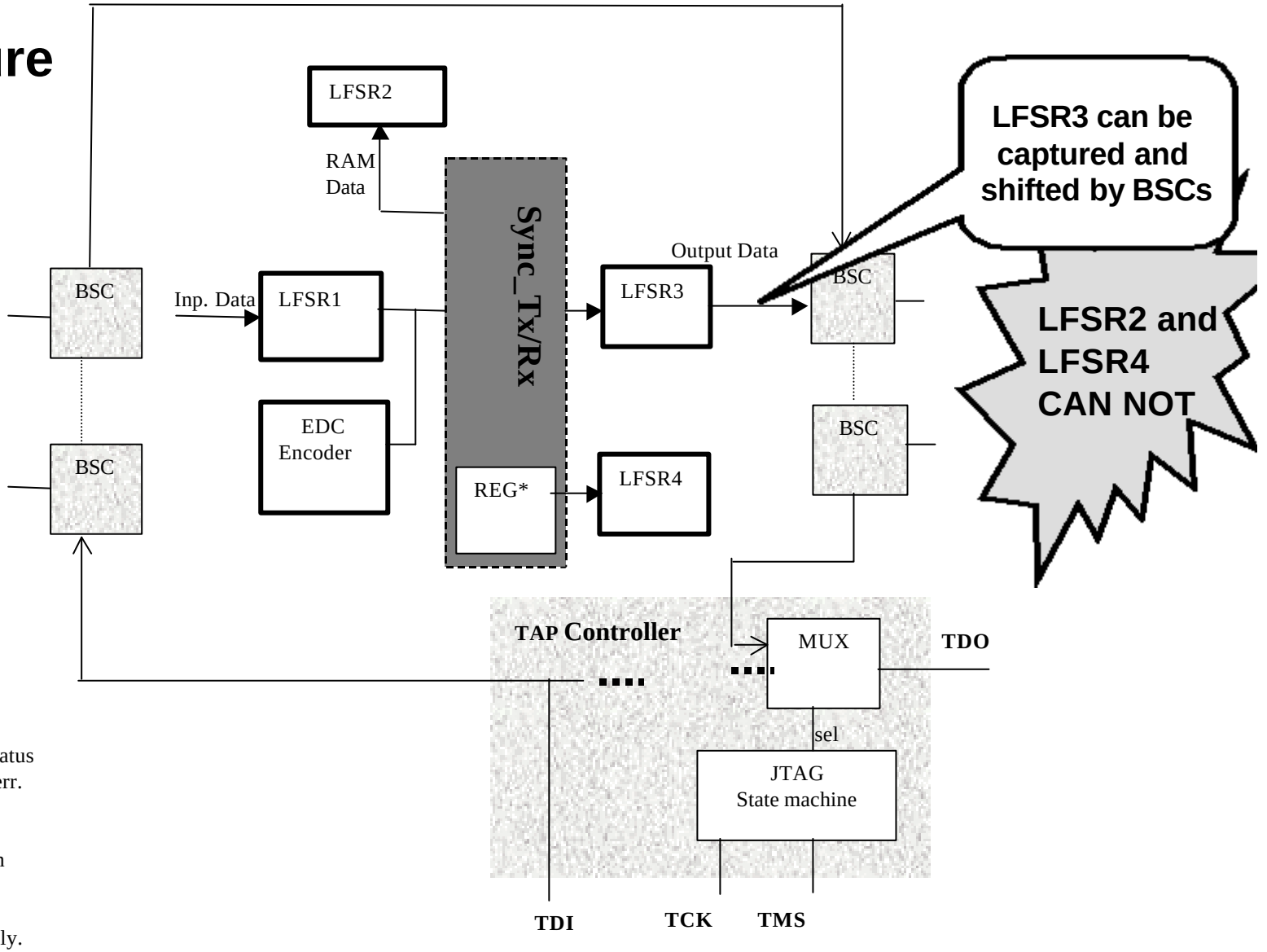
ALTERA and IEEE 1149.1



BIST solutions for ALTERA

Signature

Shift



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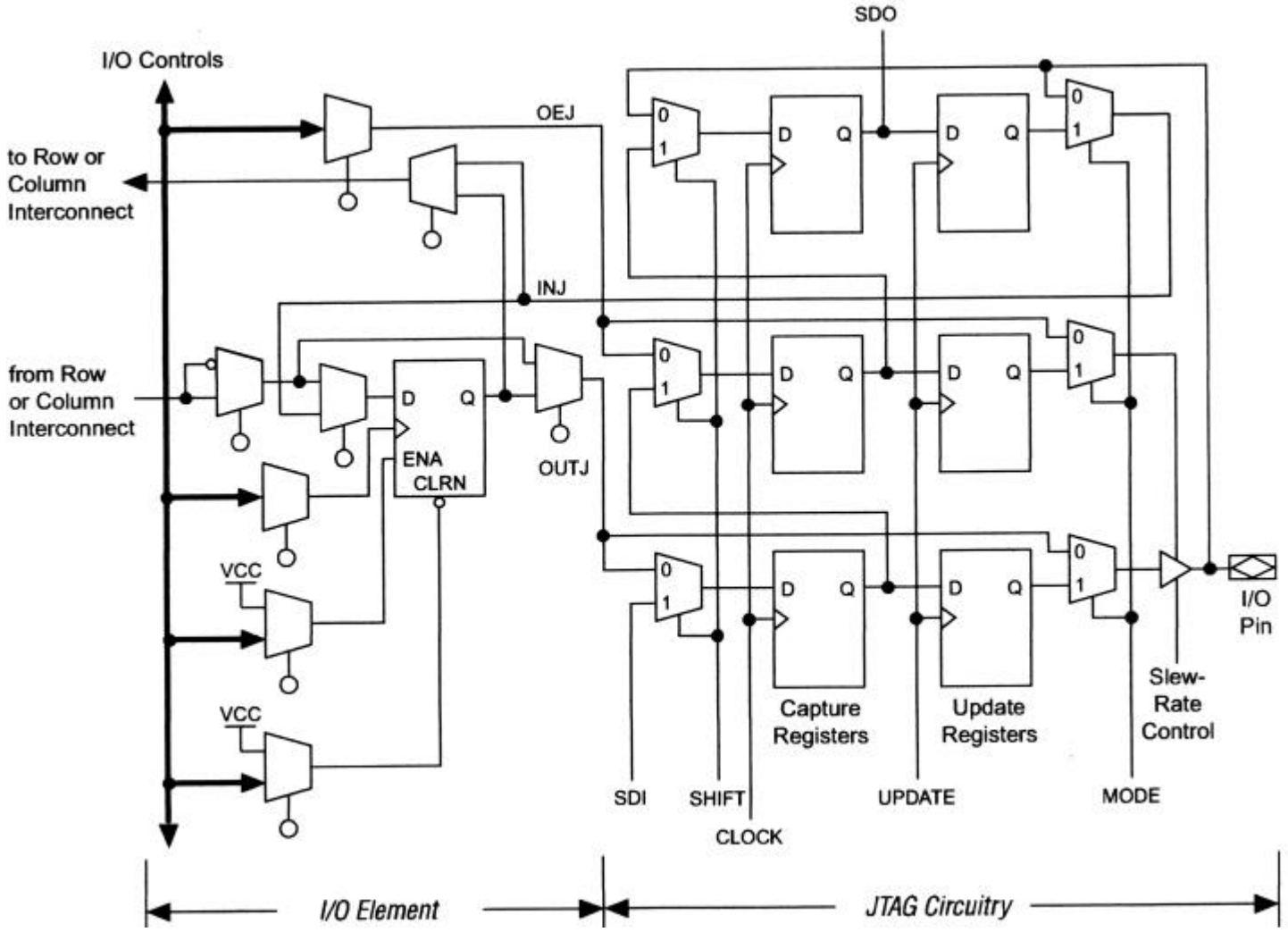
BIST solutions for ALTERA

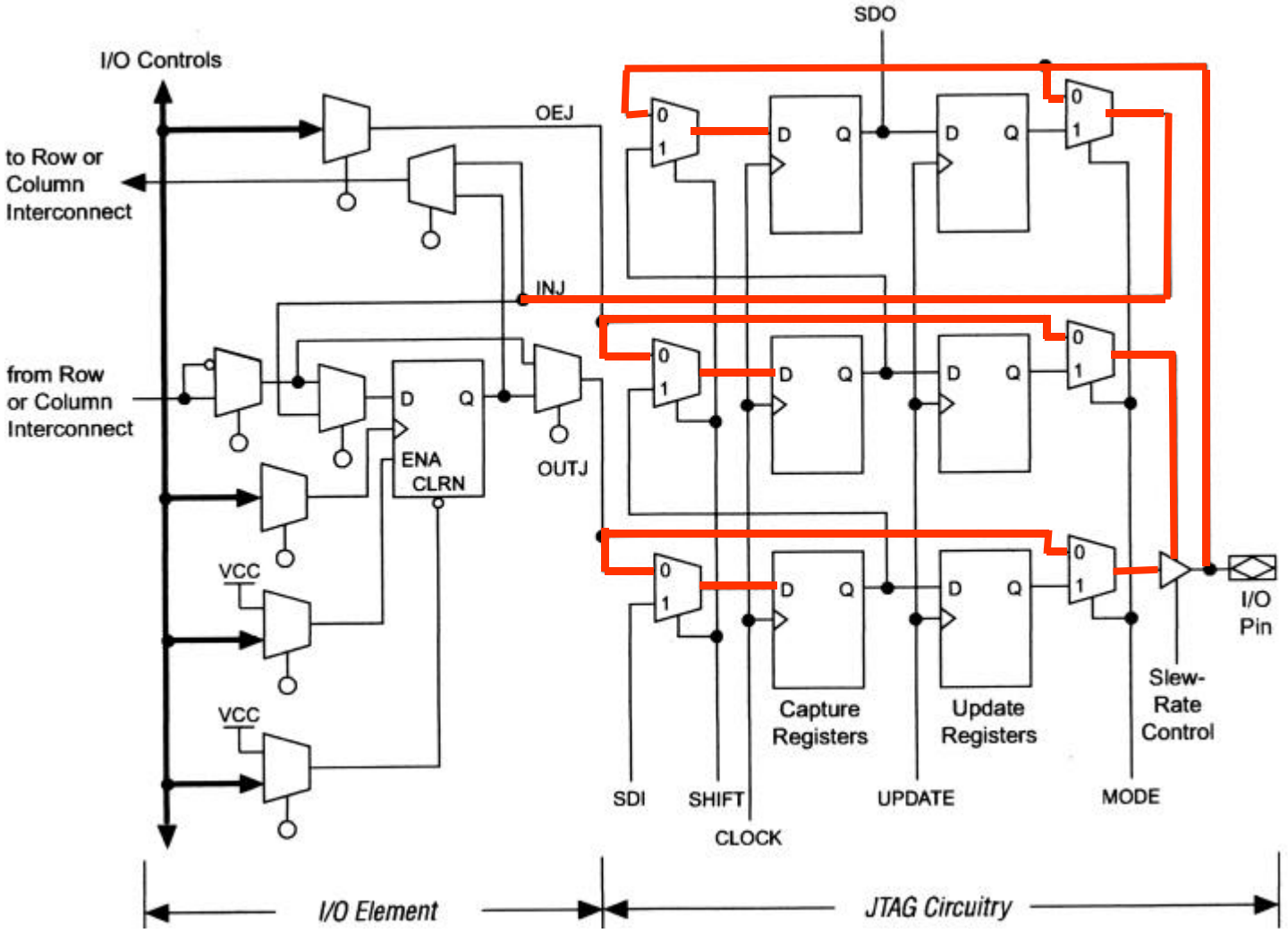
Signature Shift



I/O PIN

BIST solutions for ALTERA

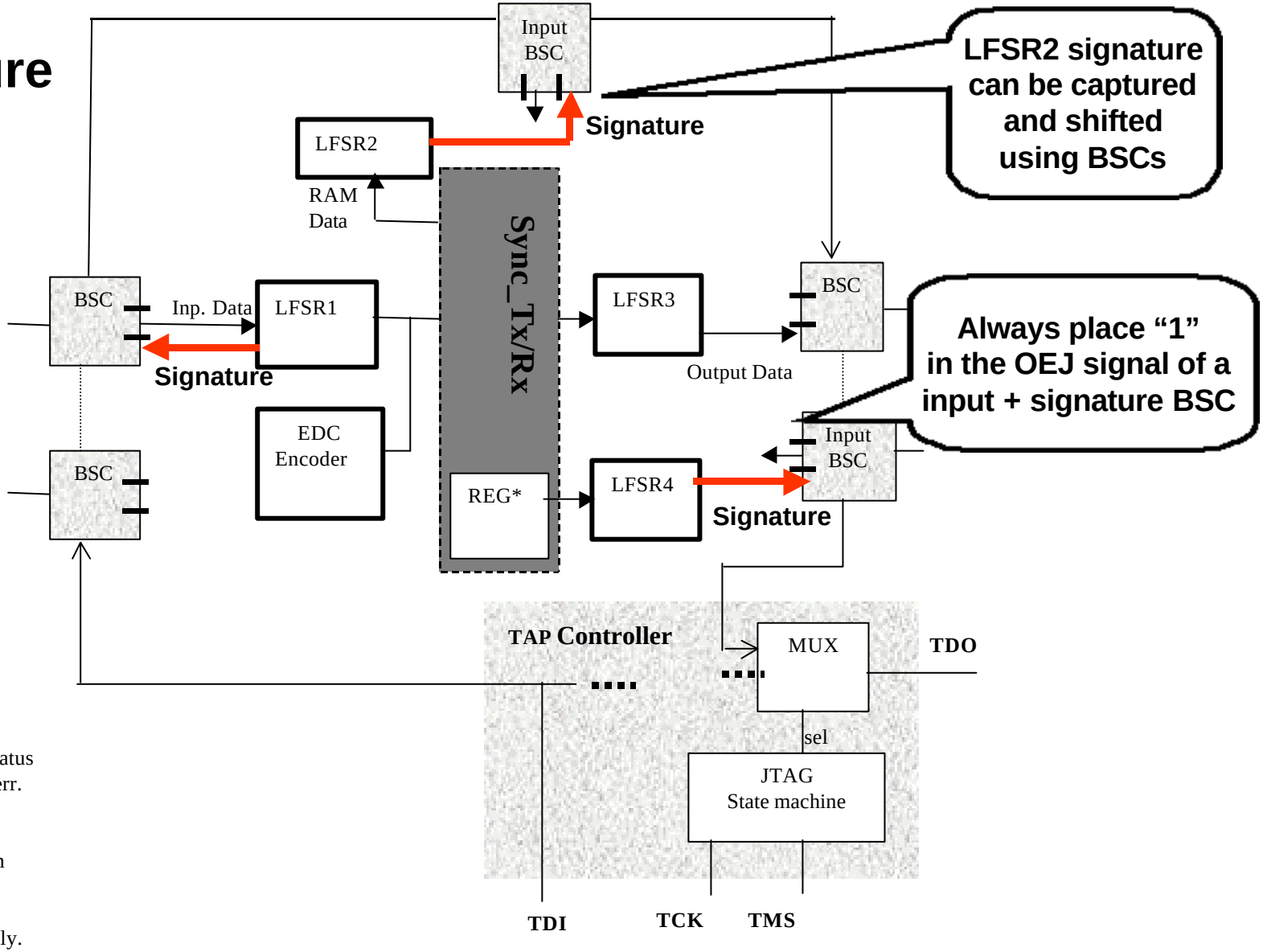
Signature Shift



SAMPLE/
PRELOAD
(Capture)

BIST solutions for ALTERA

Signature Shift



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Boundary Scan

For BIST use only.

BIST solutions for ALTERA

Start BIST Command

Available Instructions:

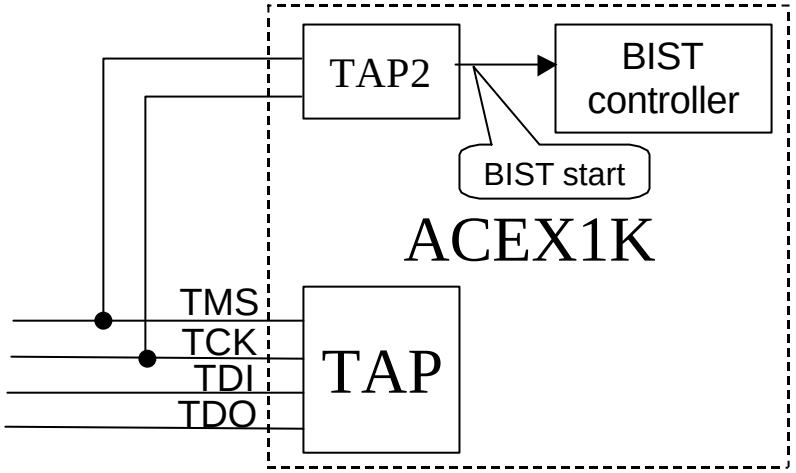
- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- IDCODE
- USERCODE

BIST solutions for ALTERA

Start BIST Command

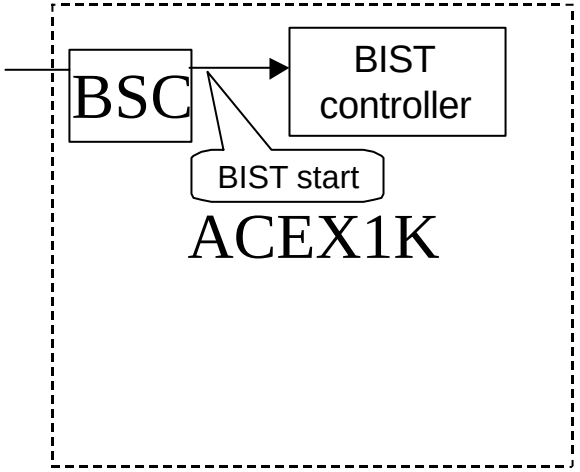
Solution 1:

Add a 2nd TAP controller state machine and decode RUNBIST



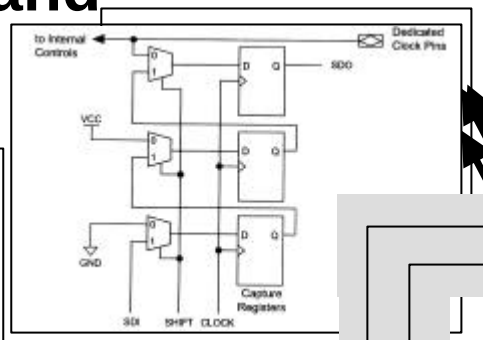
Solution 2:

Add a dedicated input pin



BIST solutions for ALTERA

Start BIST Command

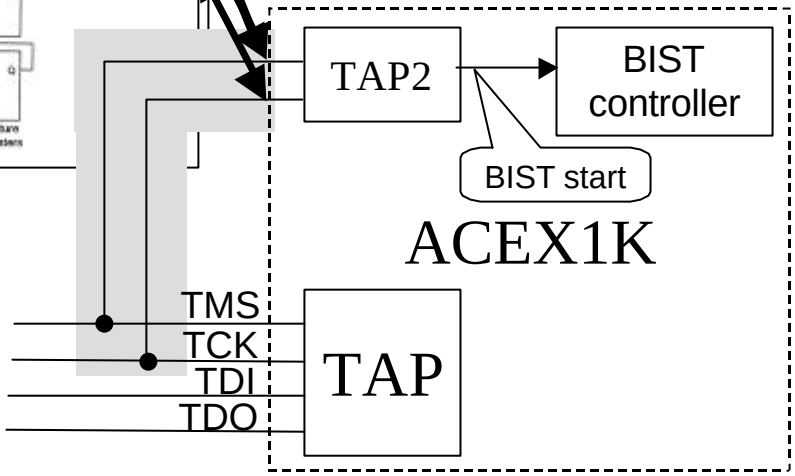


Solution 1 requires:

- **2 dedicated clock pins**
- **»100 gates TAP copy**
- **2 external connections**

Almost IEEE 1149.1

RUNBIST instruction compliant

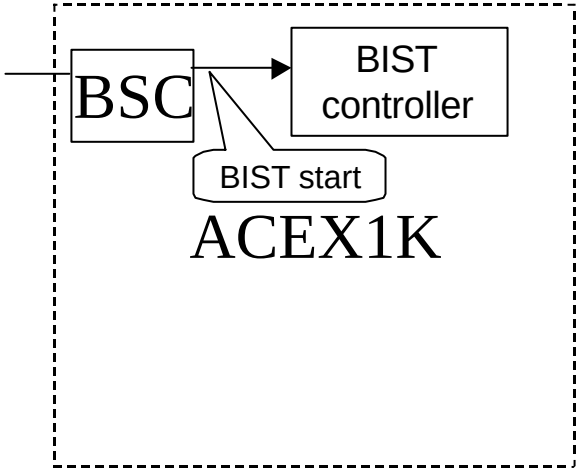


Solution 2 requires:

- **Add a dedicated input pin**

This solution is NOT IEEE 1149.1

RUNBIST instruction compliant



BIST solutions for ALTERA

Start BIST Command

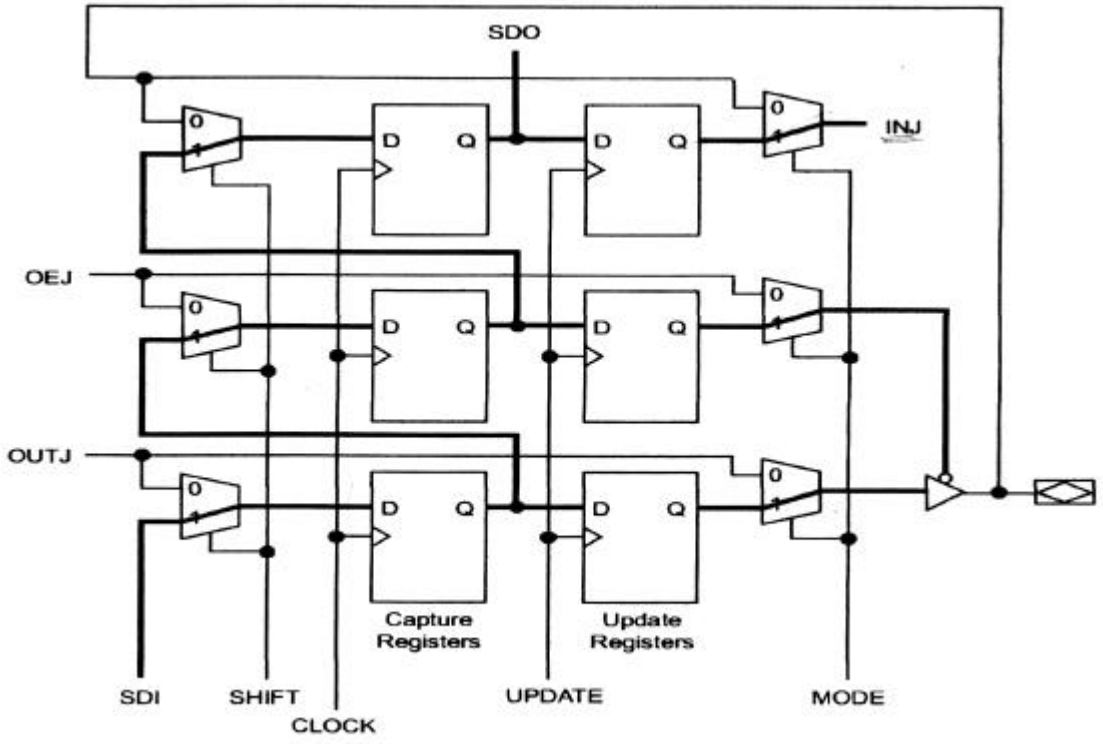
Solution 1 question:

- **What Instruction Register combination is available to use as RUNBIST ?**
  ICR (in-circuit reconfiguration) codes must be taken into account.

Solution 2 question:

- **Is it possible to start BIST using the TAP ?**

There is no INTEST instruction...



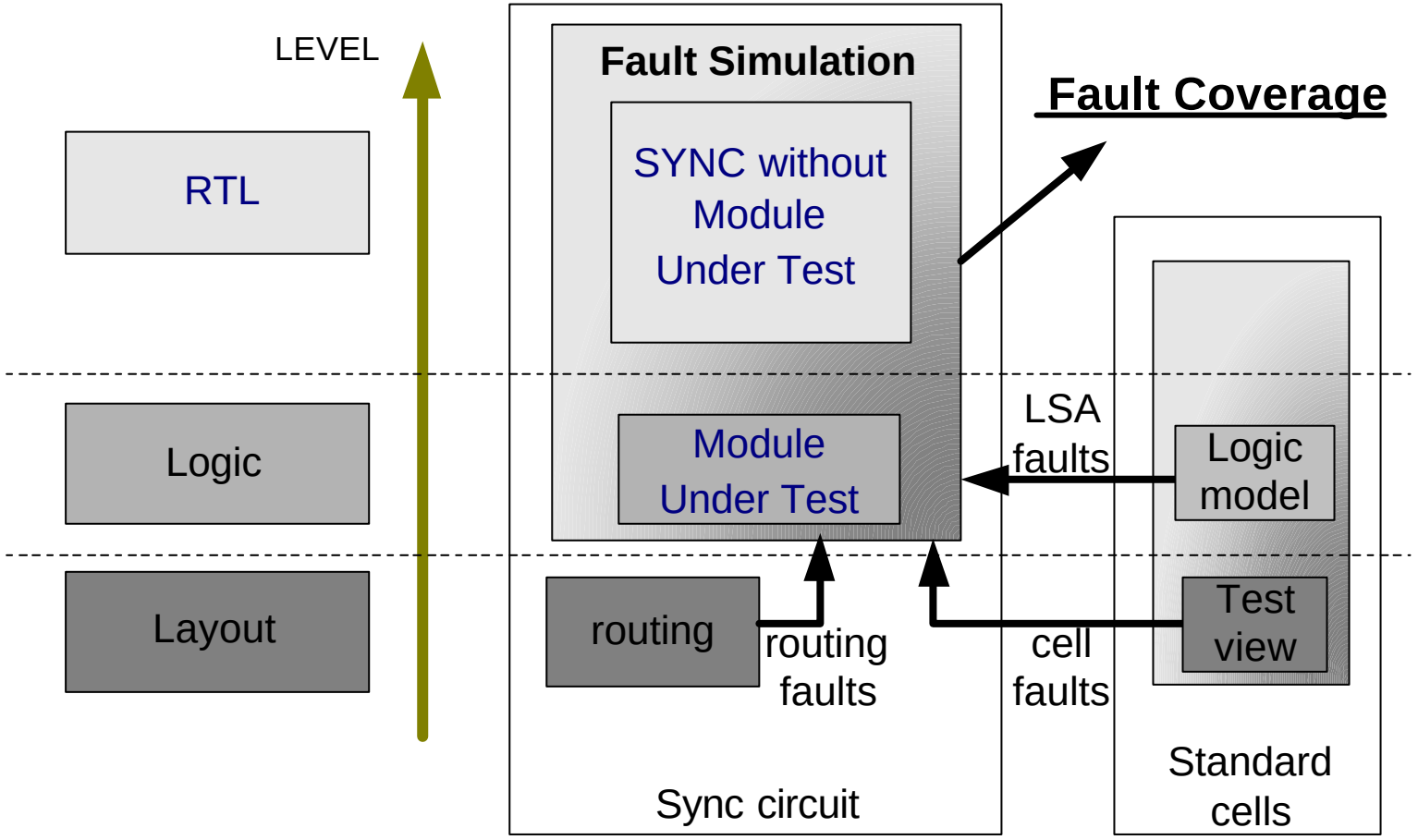
BIST Quality Evaluation

Standard-Cell Implementation:

Sync + BIST_LFSRs + BIST_control +	Tecmic RTL	INESC Logic Layout
TAP + BSCs		RTL Logic Layout

BIST Quality Evaluation

Multi-Level VeriDOS Fault Simulation



Conclusions

- **ACEX1K does not support IEEE 1149.1 compliant RUNBIST instruction;**
- **BIST Signature Shift out 100% compliant;**
- **Start BIST Command: two solutions in study;**
- **LSA/Realistic Fault coverage achieved by BIST being ascertained**