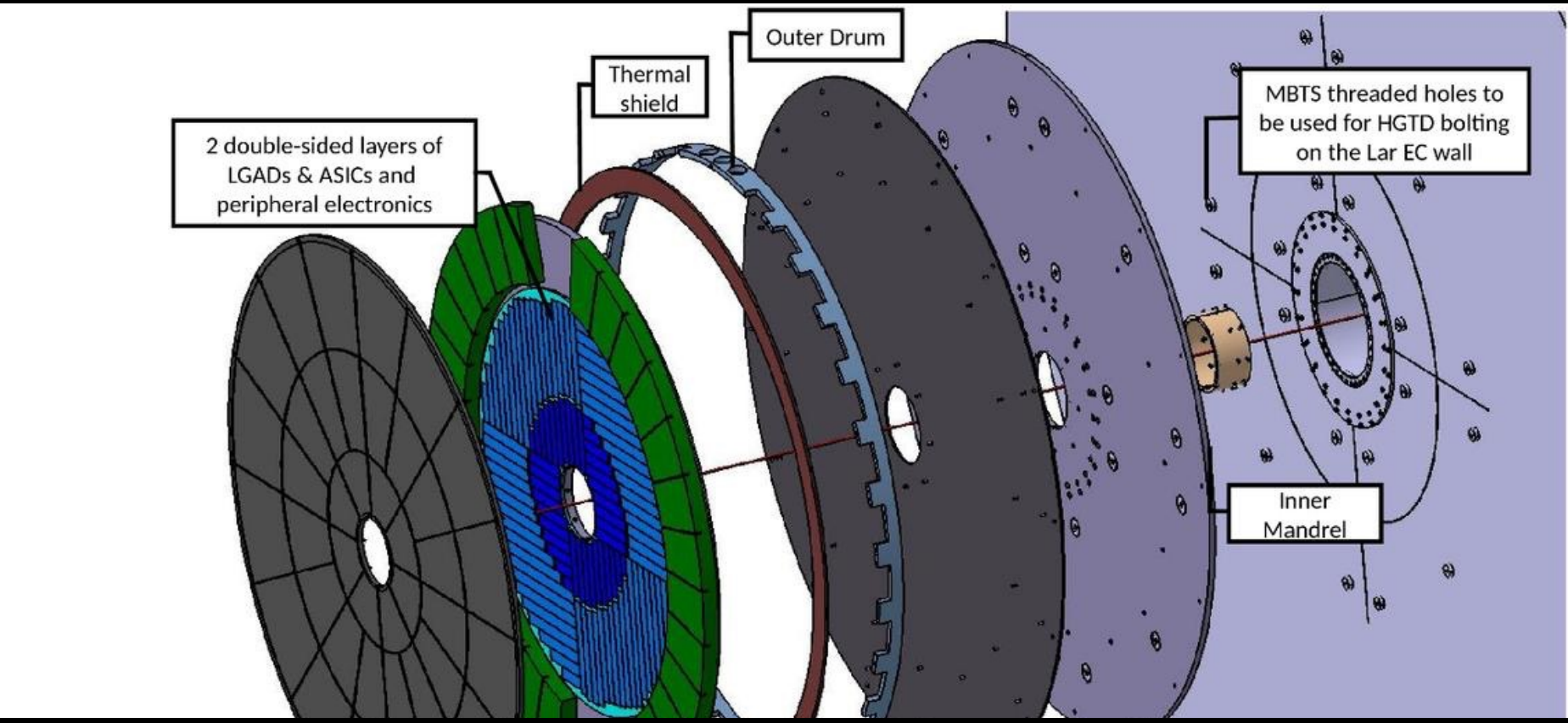
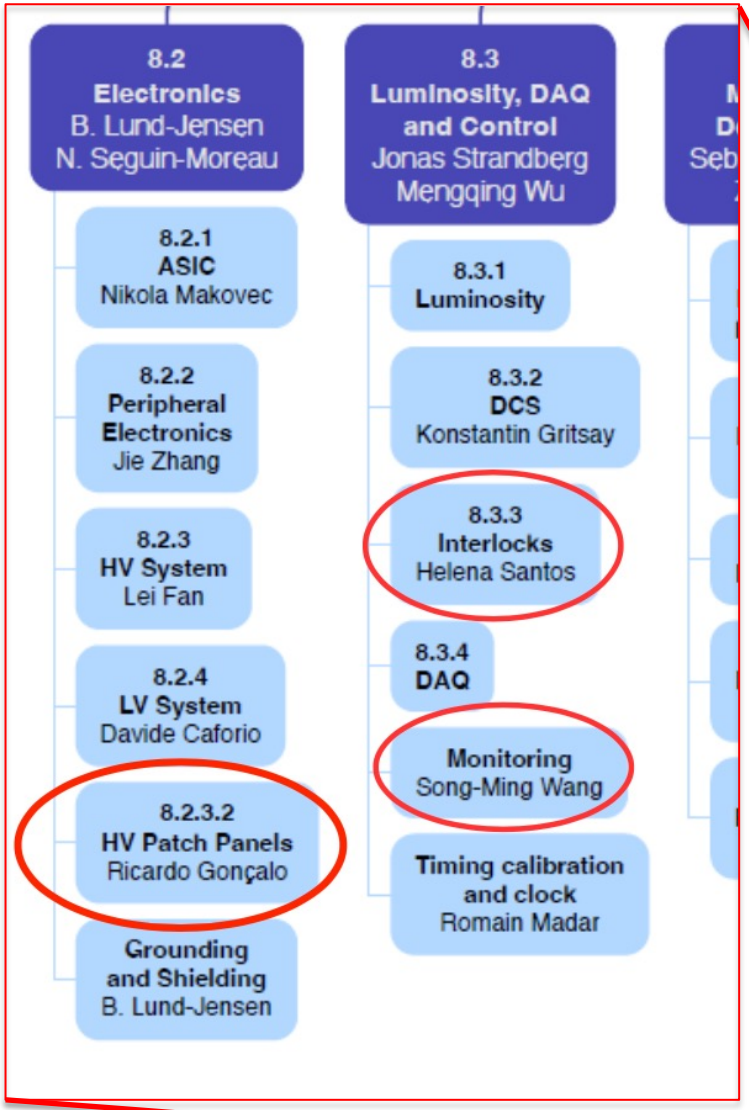
High Granularity Timing Detector

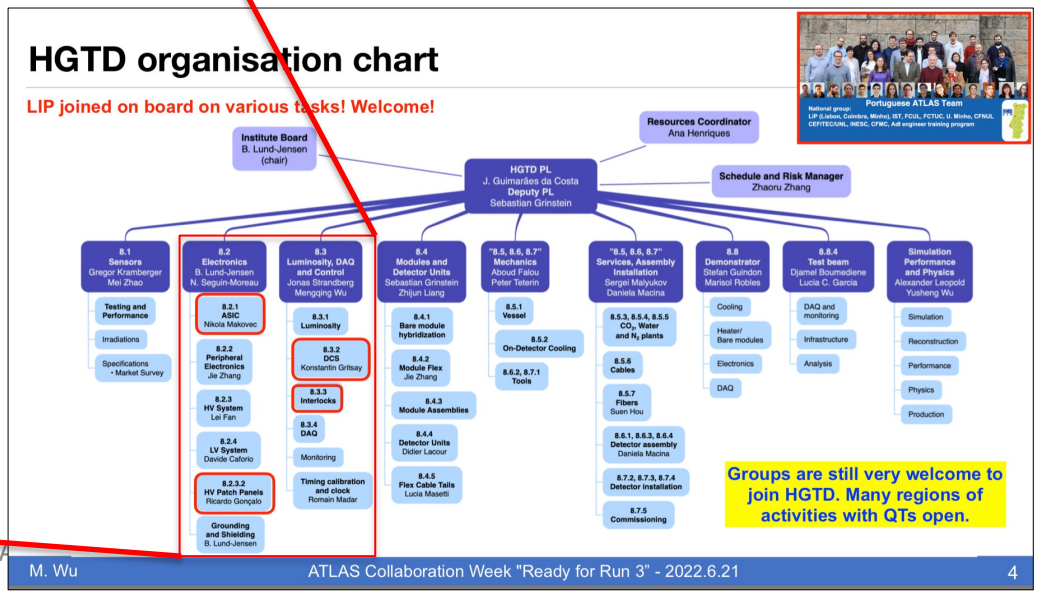


Project planning

HGTD @ LIP



- Tasks at LIP:
- Electronics Work Package:
  - High Voltage patch panels
  - ALTIROC ASIC development
- Luminosity, DAQ & Control:
  - DCS
  - Interlocks
- Infrastructure:
  - Long HV cables
  - Pigtails
  - Possibly: Mechanical design and production at LIP



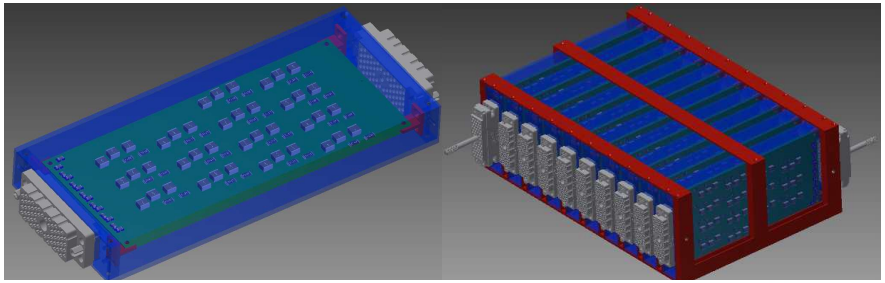
Electronics and High-Voltage

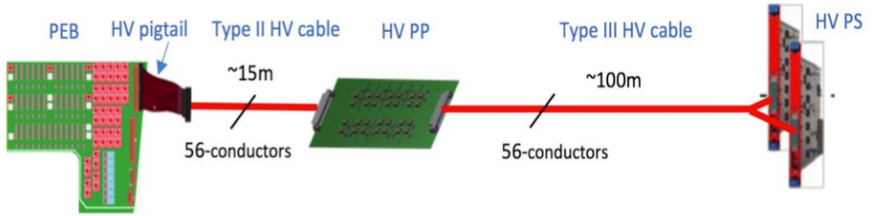
HV patch panels (António Caramelo):

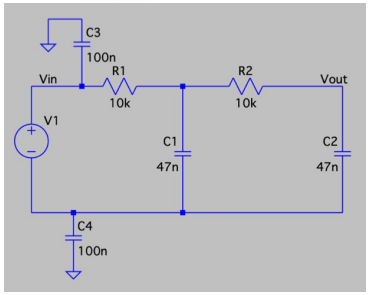
- Responsible for producing HV patch panels
- Routing and **filtering** High Voltage to HGTD detector
- Preliminary layout done and prototype tested
- Design being updated after **review**

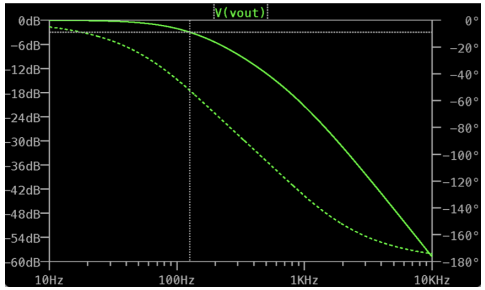
Cables:

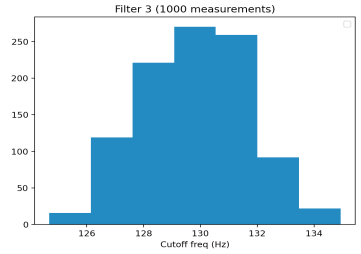
- Complicated situation: quotes > 2x original price – cannot pay for this
- Still interested in fabrication and sharing part of price
- Also interested in Pigtails

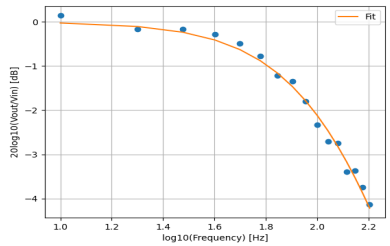


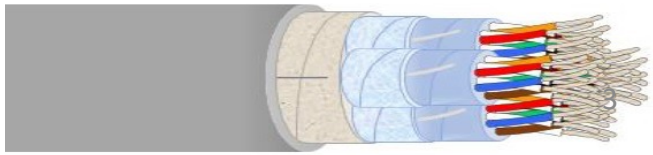








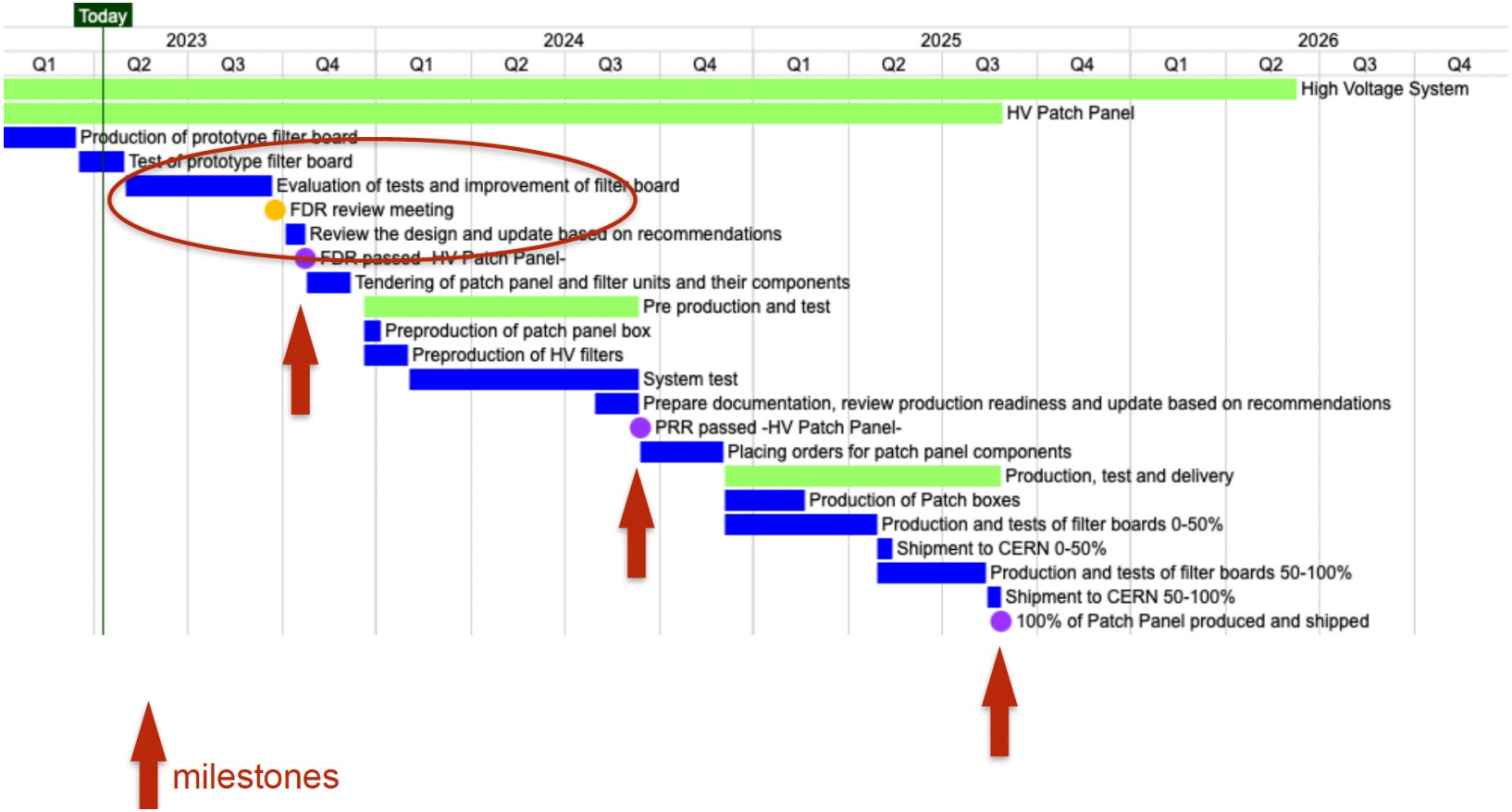




Patch panels (Electronics WP: Frank Filthaut, Jie Zhang, Nathalie Seguin-Moreau): in-kind contribution						
Task: 8.2.3.2	LIP team: Luis Lopes, Orlando Cunha, António Caramelo (P.Assis e R.Goncalo orient.)					
Timeline:	**Start**	**End**	**Months**			
Test prototype filter	20.03.23	03.05.23	1.5			
Noise tests with power supplies	02.05.23	04.08.23	3.1			
FDR	25.09.23			Provavelmente para julho		
Tendering	26.10.23	07.12.23	1.4			
Preproduction & test	20.12.23	01.02.24	1.4			
System test	02.02.24	11.09.24	7.4			
PRR	12.09.24					
Production	03.12.24	27.08.25	8.9			

Cables (Infrastructure WP - Sergei Malyukov): in-kind contribution			
Task 8.5.6	LIP team: RG		
Timeline:	**Start**	**End**	**Months**
Selecting cables and connectors:	09.06.22	30.06.23	12.9
Purchasing cables:	29.09.22	28.07.23	10.1
Rad.tests	31.07.23	20.10.23	2.7
PDR+FDR:	04.12.23		
Preproduction (cables+pigtails)	19.12.23	14.04.24	3.9
PRR	29.05.24		
Delivery of raw cables	05.09.24	16.01.25	4.4
Fabrication of cables side A	17.02.25	23.07.25	5.2
Fabrication of cables side C	24.07.25	27.11.25	4.2
Fabrication of pigtails side A	30.05.24	21.08.24	2.8
Fabrication of pigtails side C	22.08.24	14.11.24	2.8

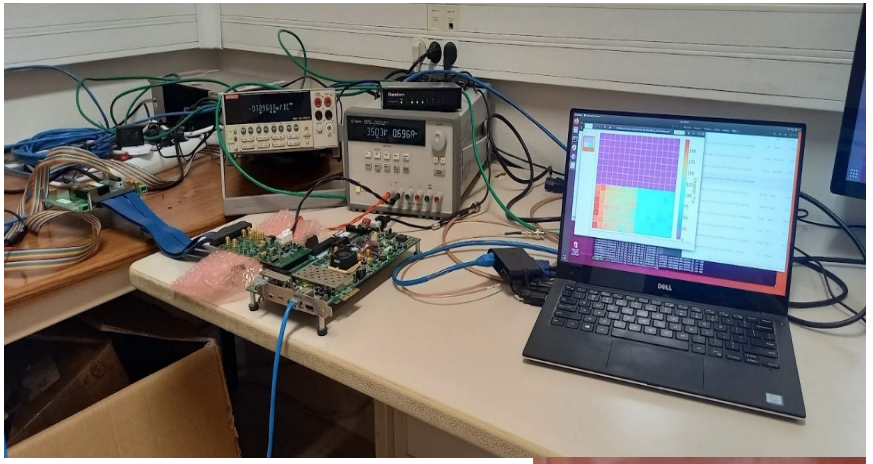
WBS 8.2.3.2 (HV patch panels): Schedule overview

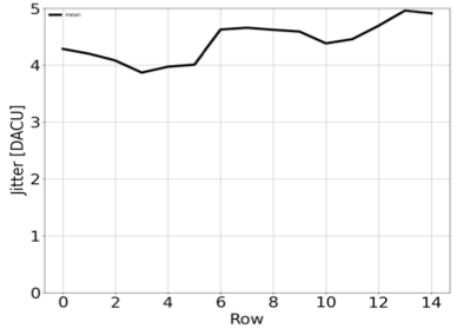


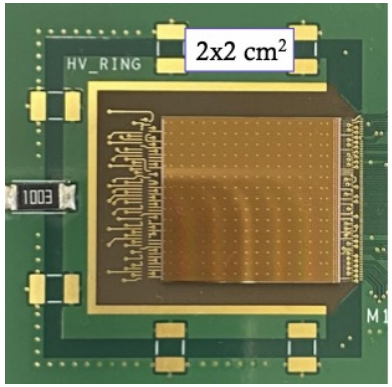
ALTIROC ASIC

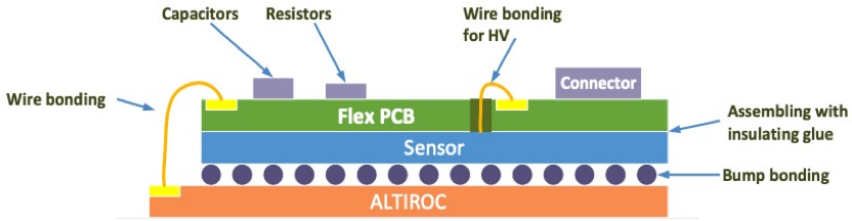
ALTIROC: (Rui Fernandez, Pedro Assis)

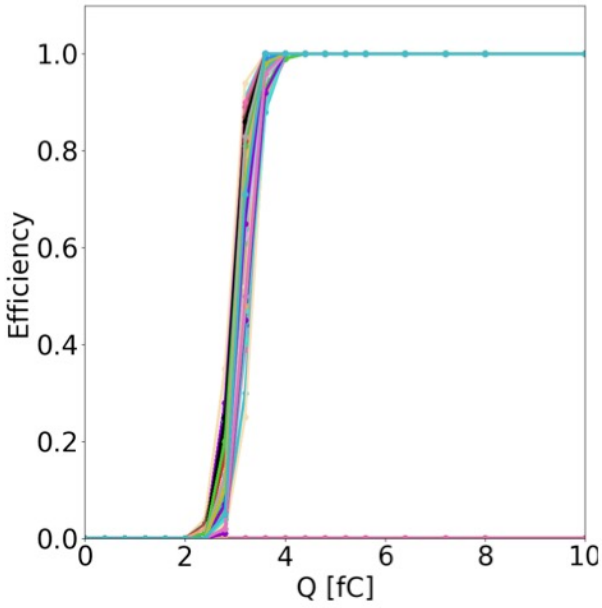
- **ASIC** under development for LGAD readout
- Taking part in ASIC **development tests**
- TID: irradiating at -35ºC – making tests now...









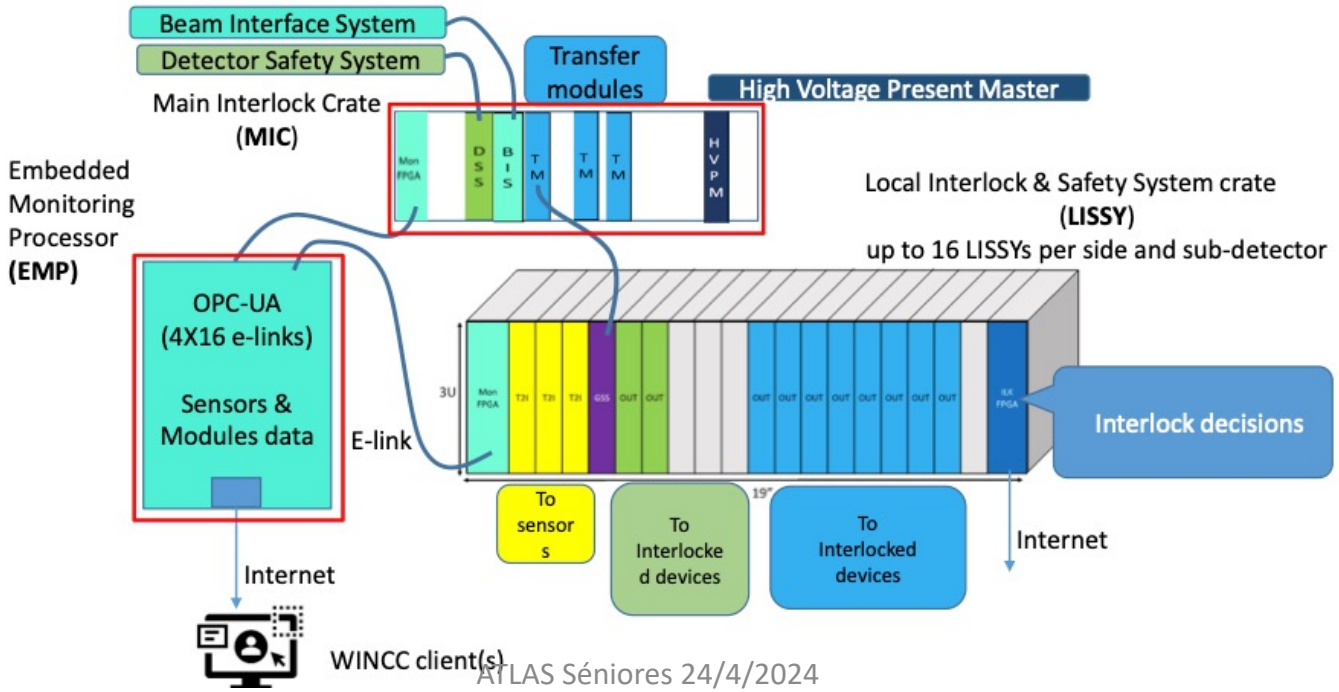


ALTIROC (Electronics WP: Frank Filthaut, Jie Zhang, Nathalie Seguin-Moreau): developemnt						
Task: 8.2.1	LIP team: Rui Fernandez, P.Assis, Miguel Ferreira					
Timeline:	**Start**	**End**	**Months**			
Altiroc3 characterisation: functio	24.04.23	15.08.23	3.8			
Irradiation tests (TID)	19.05.23	15.08.23	2.9			
Measurements continuation	16.08.23	14.02.24	6.1			

DCS and Interlocks

- **Detector Control System** (Rui Fernandez, Filipe Martins):
  - Contributing to DCS architecture definition
  - Readout of DCS environment data through ELMB2 communication board

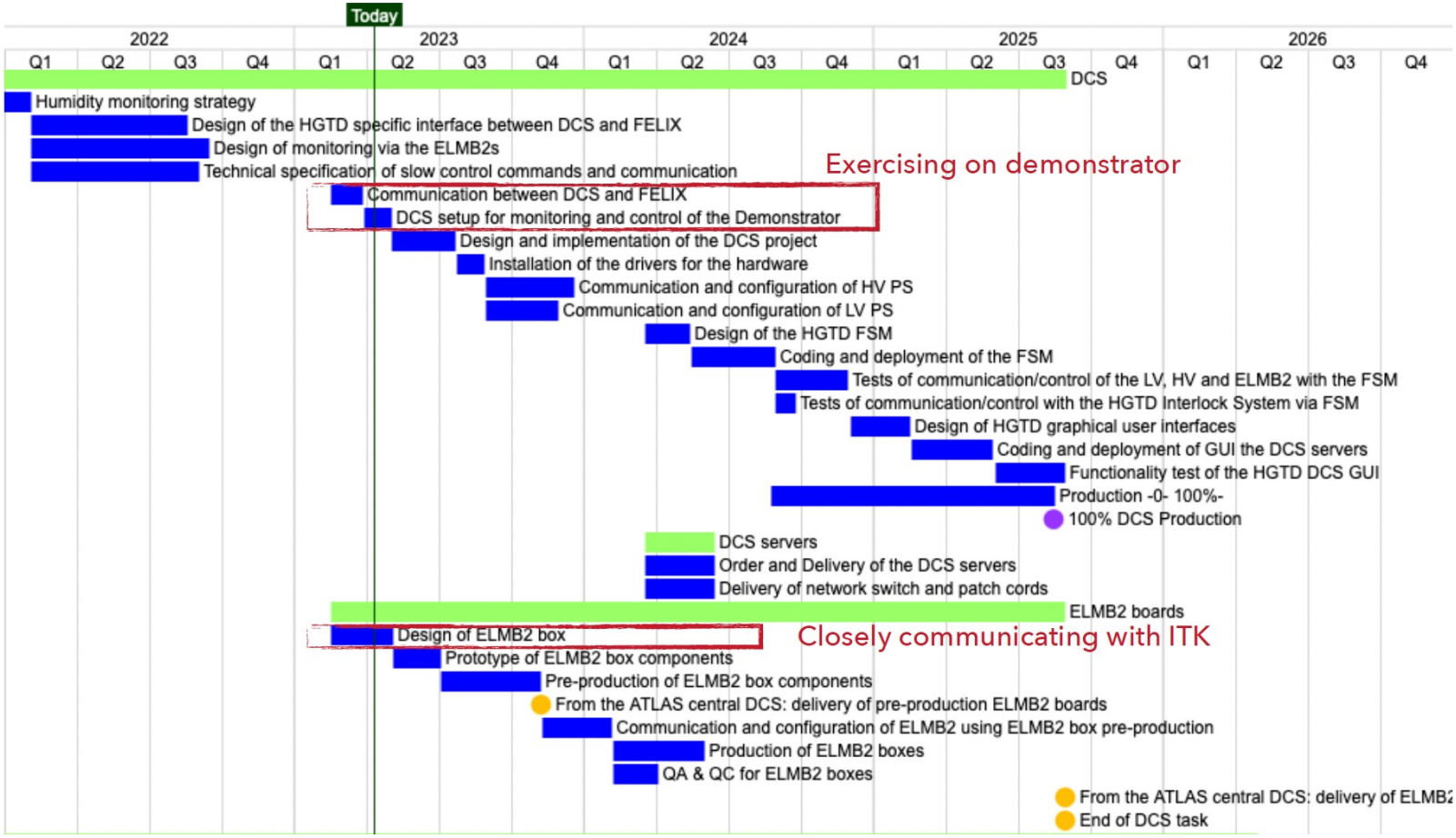
- **Interlocks** (Helena, Maria Cruz):
  - Responsability for HGTD Interlocks – mostly will re-use ITk design
    - Likely to produce an interlock module ourselves (HV-Present)



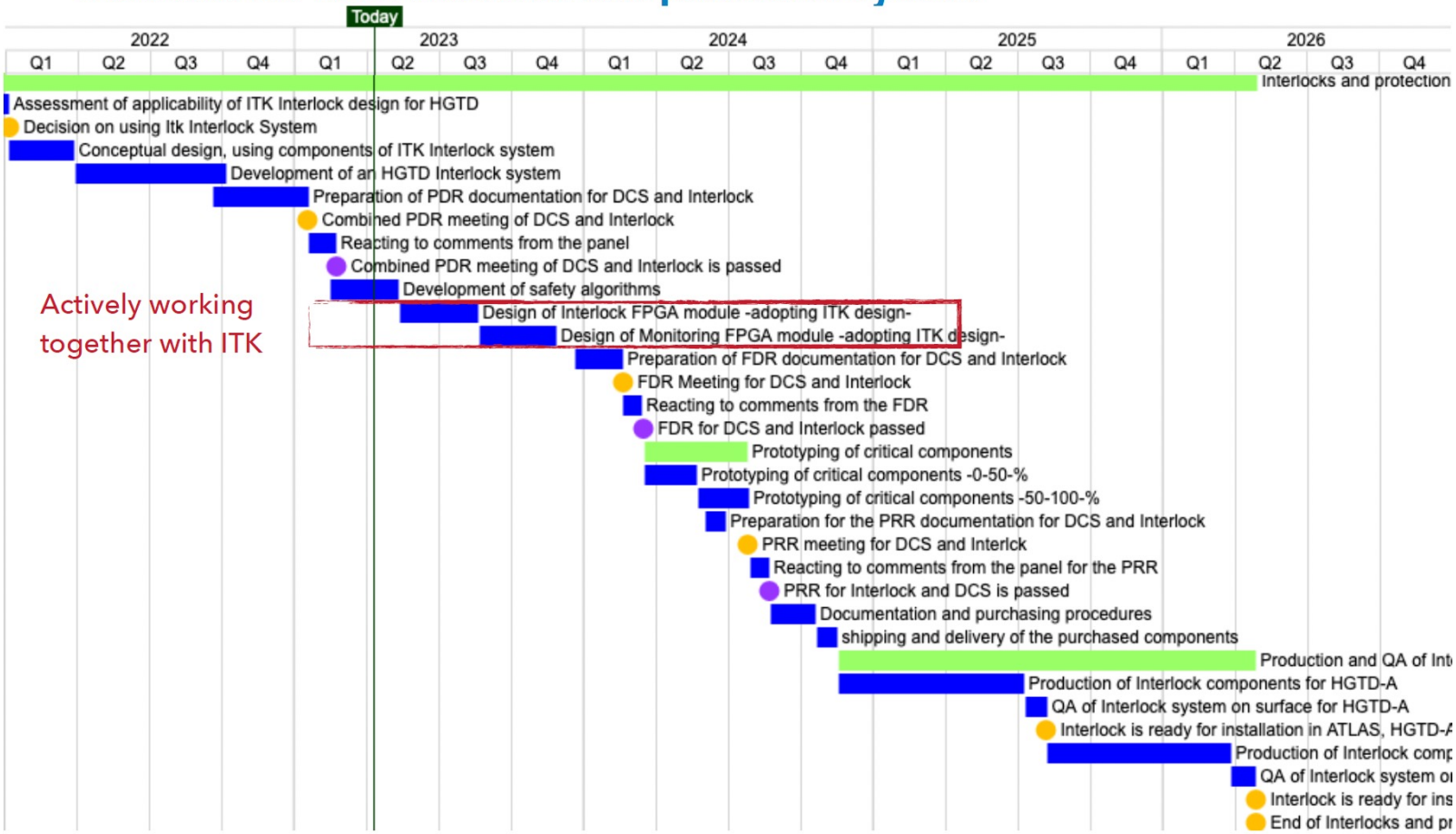
Interlocks (Lumi, DAQ & Control WP: Jonas Strandberg, Mengqing Wu): development & in-kind contribution						
Task: 8.3.3	LIP team: Helena Santos, Maria Cruz (P.Assis e R.Goncalo orient.)					
Timeline:	**Start**	**End**	**Months**			
Development of safety algorithm	15.02.23	12.05.23	2.9			
Design of interlock FPGA module	15.05.23	21.08.23	3.3			
Prototyping of critical component	18.03.24	26.07.24	4.3			
Production & QA	18.11.24	27.04.26	17.5			

DCS (Lumi, DAQ & Control WP: Jonas Strandberg, Mengqing Wu): development & in-kind contribution						
Task: 8.3.2	LIP team: Rui Fernandez (com P.Assis, Miguel Ferreira), Filipe Martins					
Timeline:	**Start**	**End**	**Months**			
ELMB2 box design	15.02.23	04.05.23	2.6			
ELMB2 box prototype	05.05.23	04.07.23	2.0			
ELMB2 box pre-production	05.07.23	08.11.23	4.2			
FDR (DCS+Interlock)	19.02.24					
PRR (DCS+Interlock)	22.08.24					
Purchase of DCS servers & Switch	18.03.24	14.06.24	2.9			
Production & QA	23.08.24	15.08.25	11.9			

Schedule for 8.3.2 DCS



Schedule for 8.3.3 Interlock and protection system



	Patch panels	ALTIROC	DCS	Interlocks	Cables & pigtails
Budget:	83k		16k	35k	64k pigtails + 34k HV cable fabrication + 160k raw HV cables
Peak expenditure	2024		2024	2024	2023
Apr.23	test prototype			Development of algorithm	Selecting cables & connectors
May.23	test w/ power supp.(CERN)	Altiroc3 characterisation	ELMB2 box prototype	Design FPGA module	
Jun.23		Irradiation tests			
Jul.23	FDR		ELMB2 box pre-production		**Cables purchased**
Oct.23	**tendering**				
Dec.23	**preproduction**				Preproduction
Feb.24	system test		FDR		
Mar.24			Purchase of servers & s	Proototyping of critical items	
May.24					PRR & Pigtail production
Sep.24	PRR		**PRR & Production**		
Dec.24	**Production**			**Production & QA**	
Feb.25					Cable fabrication
Jul.25					

MoU item	PBS	MoU item	CORE (kCHF)	% of CORE	Total	Contribution	Obs.
Patch panels	8.2.3.2	Patch panels	82.8	100	82.8	Design and p	Agreed with CERN
DCS	8.3.2	DCS	33	100	33.0	Contribution	to purchase, development
DCS servers	8.3.2.1	DCS servers	16.1	100	**16.1**		
Interlocks	8.3.3	Interlocks	35	100	35.0	Contribution	to purchase, development
Raw cables (short -	8.5.6.1.2	Raw cables (short - proxin	20	0	0.0	procurement	cost from BoE
Connector 1	8.5.6.2.3	Connector 1	8.5	0	0.0	procurement	cost from BoE
Connector 2	8.5.6.2.4	Connector 2	25.6	0	0.0	procurement	cost from BoE
Cable fabrication	8.5.6.4.2	Cable fabrication	64	0	0.0		cost from BoE
Raw cables (long)	8.5.6.1.9	Raw cables (long)	160	100	160.0	procurement	cost from BoE
Connector 1	8.5.6.2.17	Connector 1	10.2	100	10.2	procurement	cost from BoE
Connector 2	8.5.6.2.18	Connector 2	17	100	17.0	procurement	cost from BoE
Cable fabrication	8.5.6.4.9	Cable fabrication	34	100	34.0		cost from BoE
HV pigtails	8.5.6.3.1	HV pigtails	64	100	64.0		
					452.1		