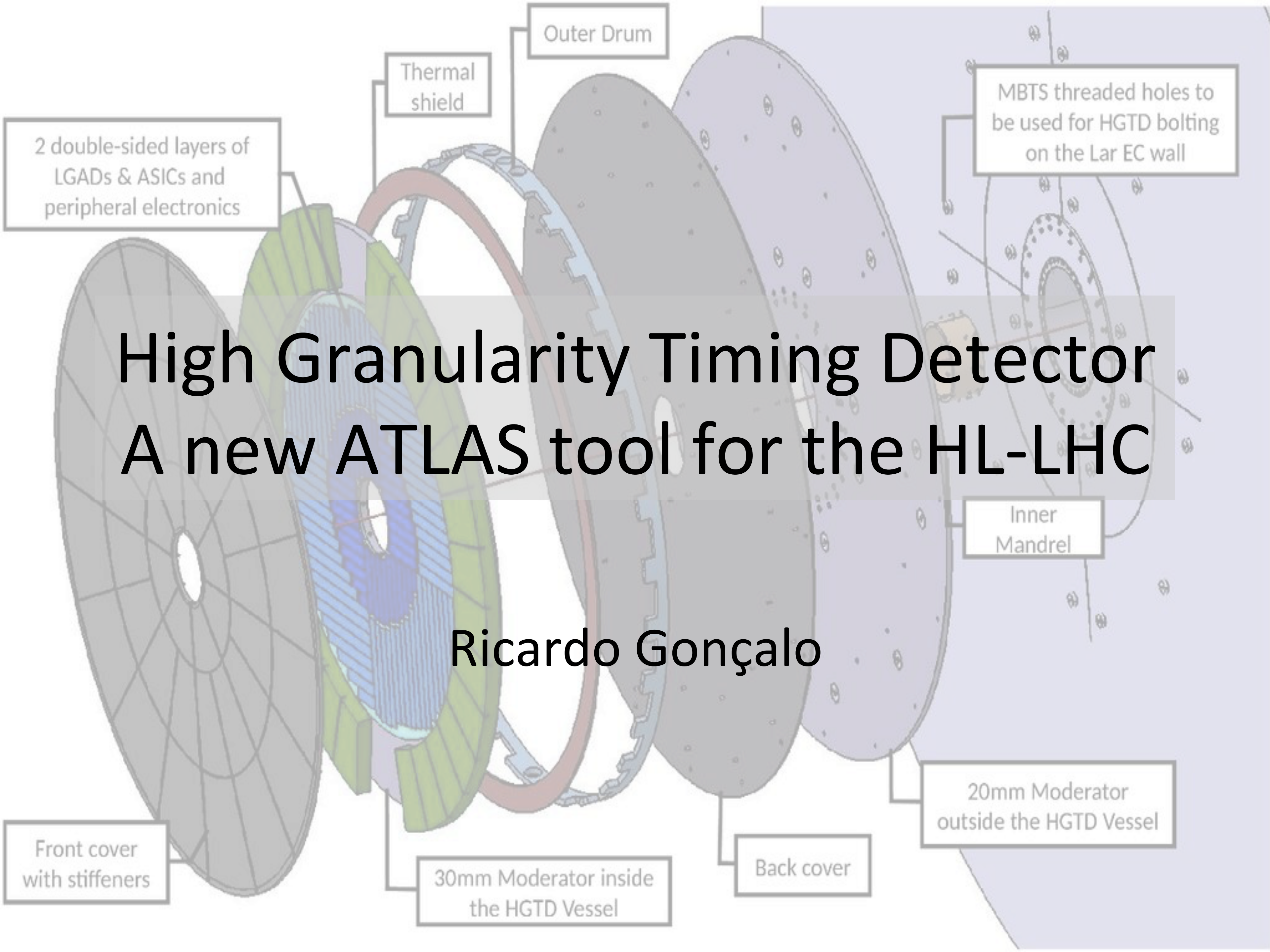
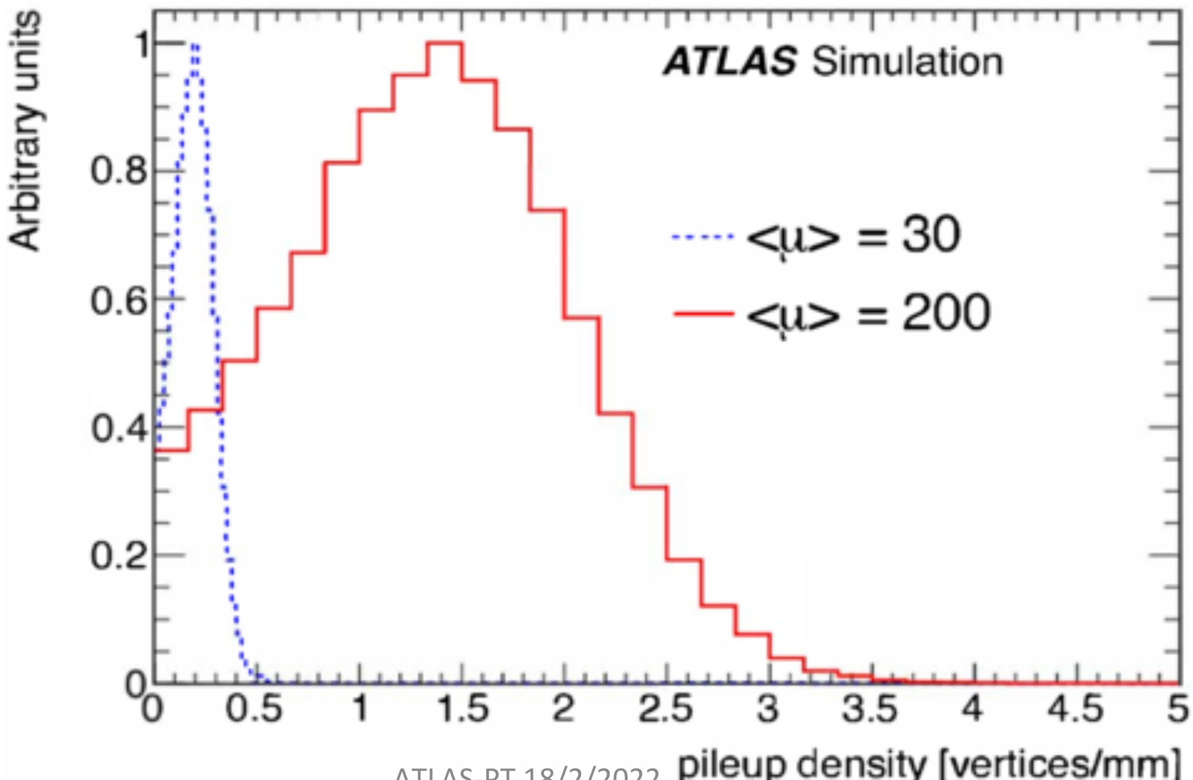
High Granularity Timing Detector
A new ATLAS tool for the HL-LHC

Ricardo Gonçalo



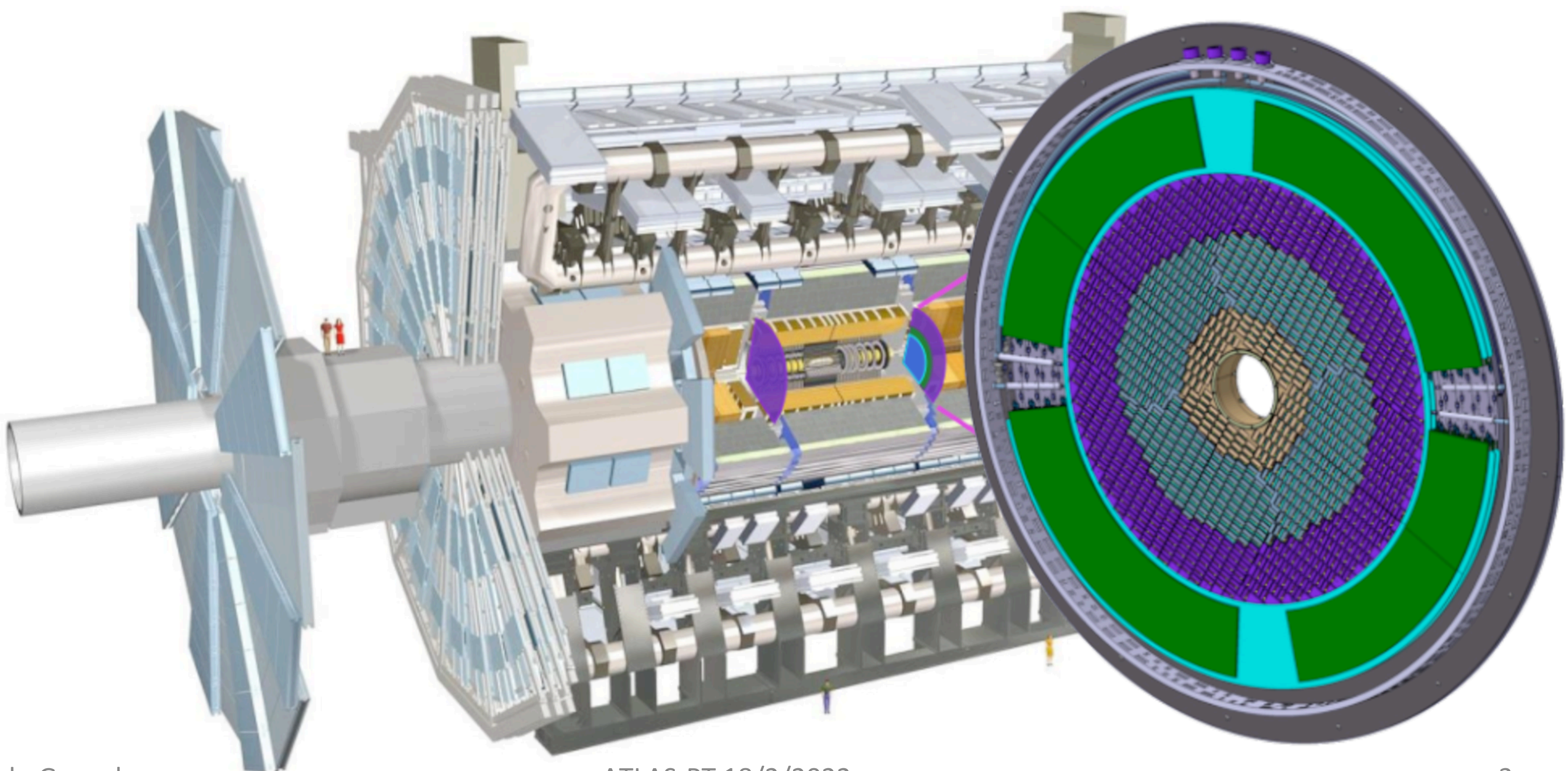
High-Luminosity LHC

- The price of high luminosity →high pileup
- At the HL-LHC we expect a maximum <μ> of around 200
- Average collision density of 1.8 vertices / mm
- How to deal with these extreme conditions?



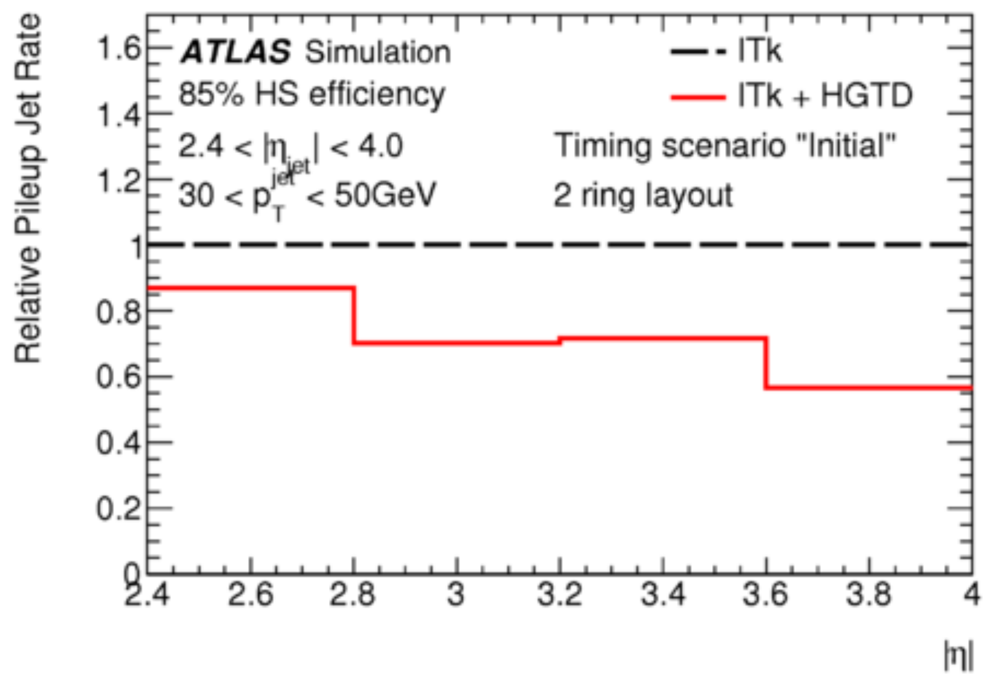
Tracking and the HGTD

- The Inner Tracker (Itk) will replace current ID
  - Coverage extended from $|\eta|<2.5$ to $|\eta|<4$
- The HGTD will add timing information to tracks
  - Upgrade ATLAS tracking **from 3-D to 4-D tracking sys**tem (ITK+HGTD)



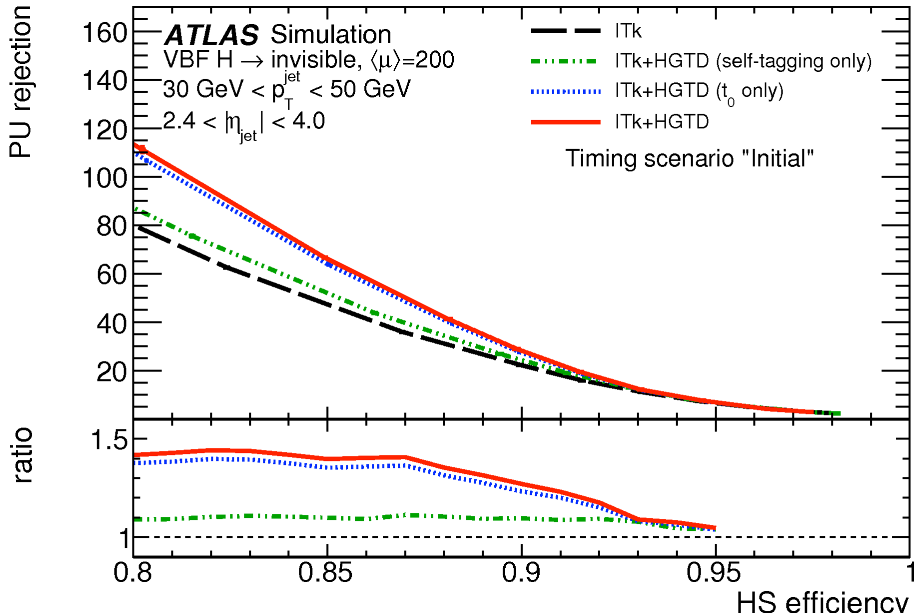
Pileup mitigation and luminosity

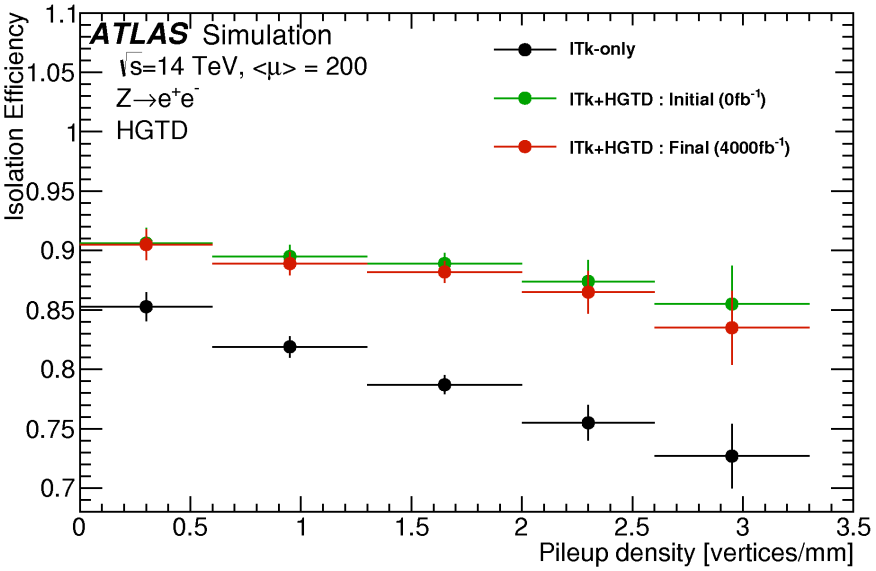
- ITk has good σ_Z resolution for central rapidity
  - Allow good separation between vertices
- Timing information will be important for large $|\eta|$ where σ_Z is worse
- Will also greatly improve luminosity measurement with hit rate cunting



Impact on reconstruction

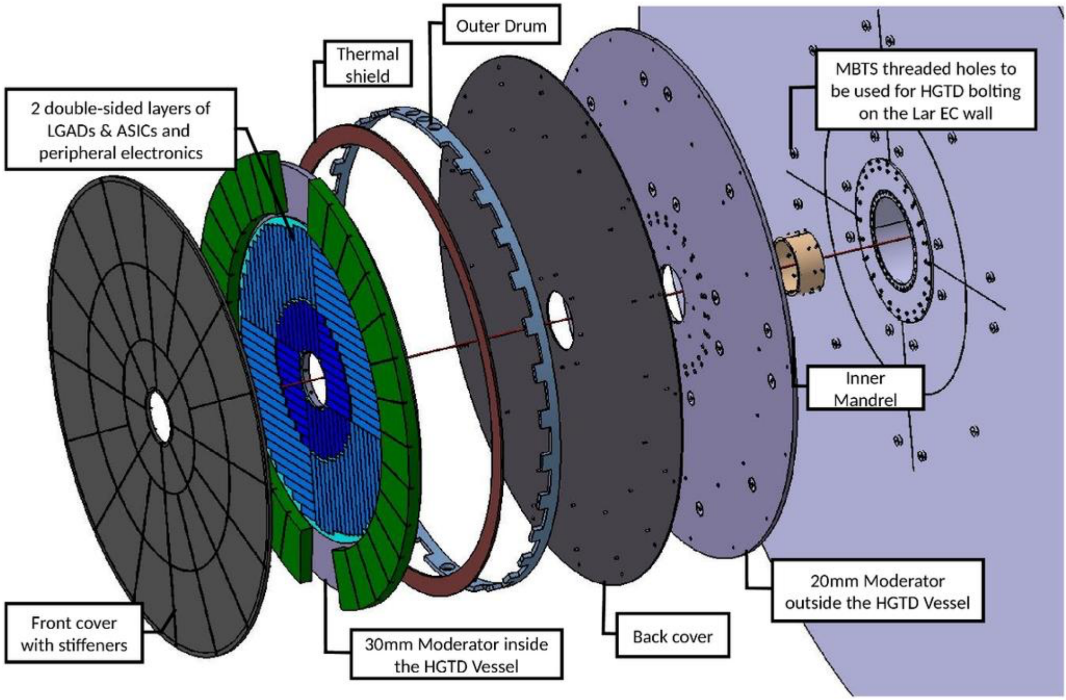
- Pileup-jet rejection increases by a factor of 1.4 (for 85% efficiency)
- Lepton isolation efficiency increases up to 25 %
  - HGTD removes majority of pileup deterioration

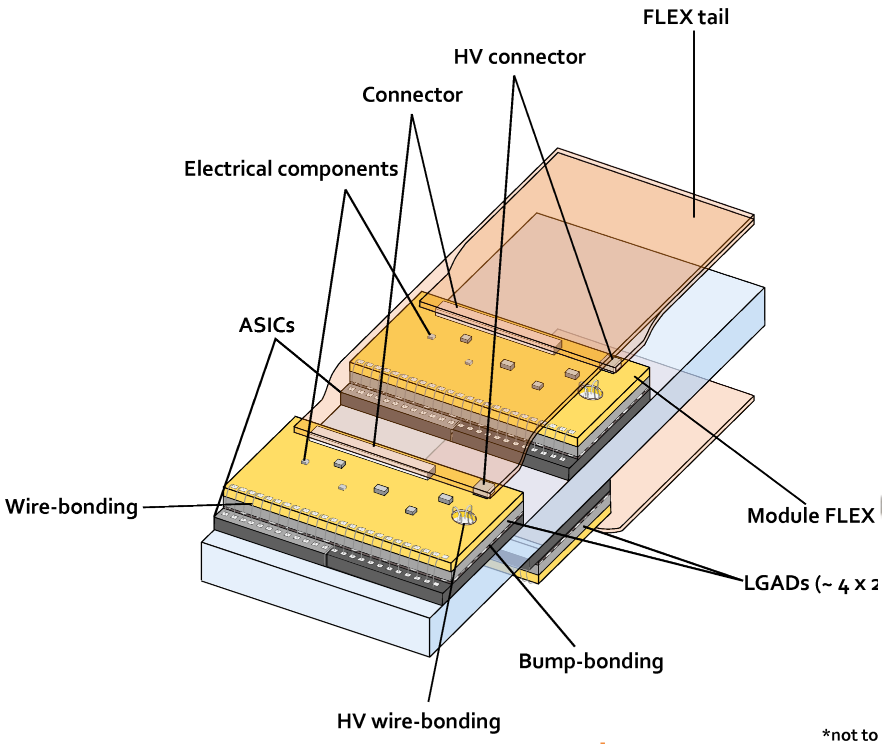


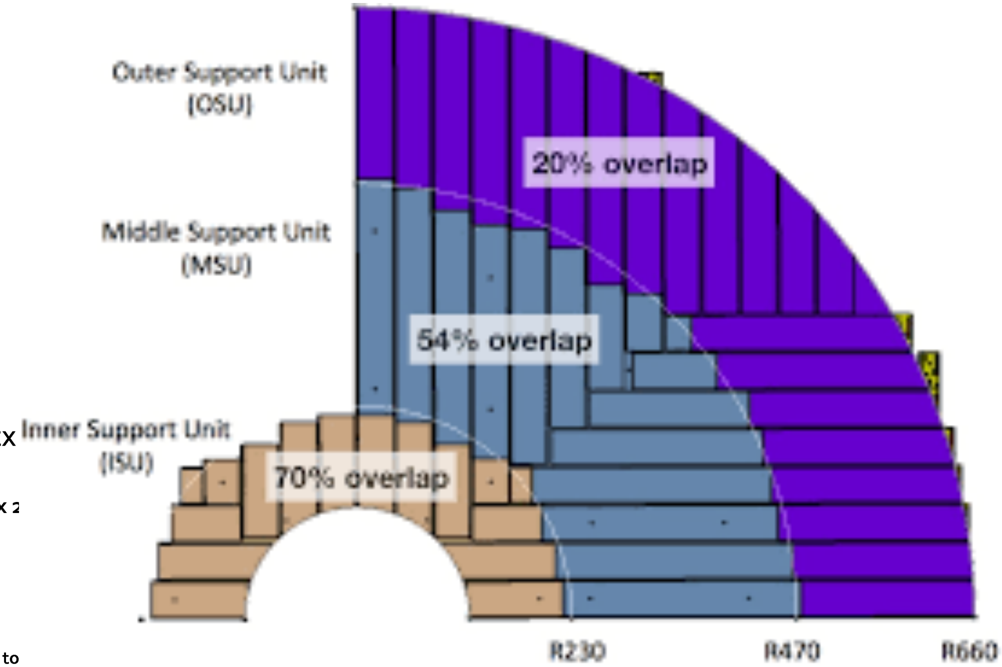


High Granularity Timing Detector

- Two instrumented double-sided layers
- 7.5 mm-thick, three rings mounted in two cooling disks
- Gap region between the barrel and the end-cap calorimeter at z=3.5m from interaction point
- High-precision time measurement: 30 - 50 ps resolution per track
- Assign time to tracks in the forward region: $2.4 < \eta < 4.0$
- Improve pileup rejection by a factor of 6 and correct track-to-vertex association



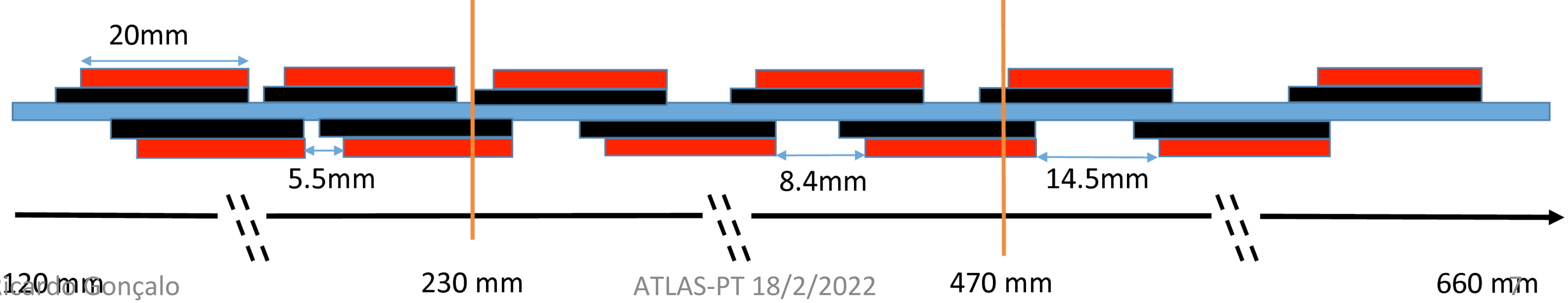




Inner Ring:
70% sensor overlap

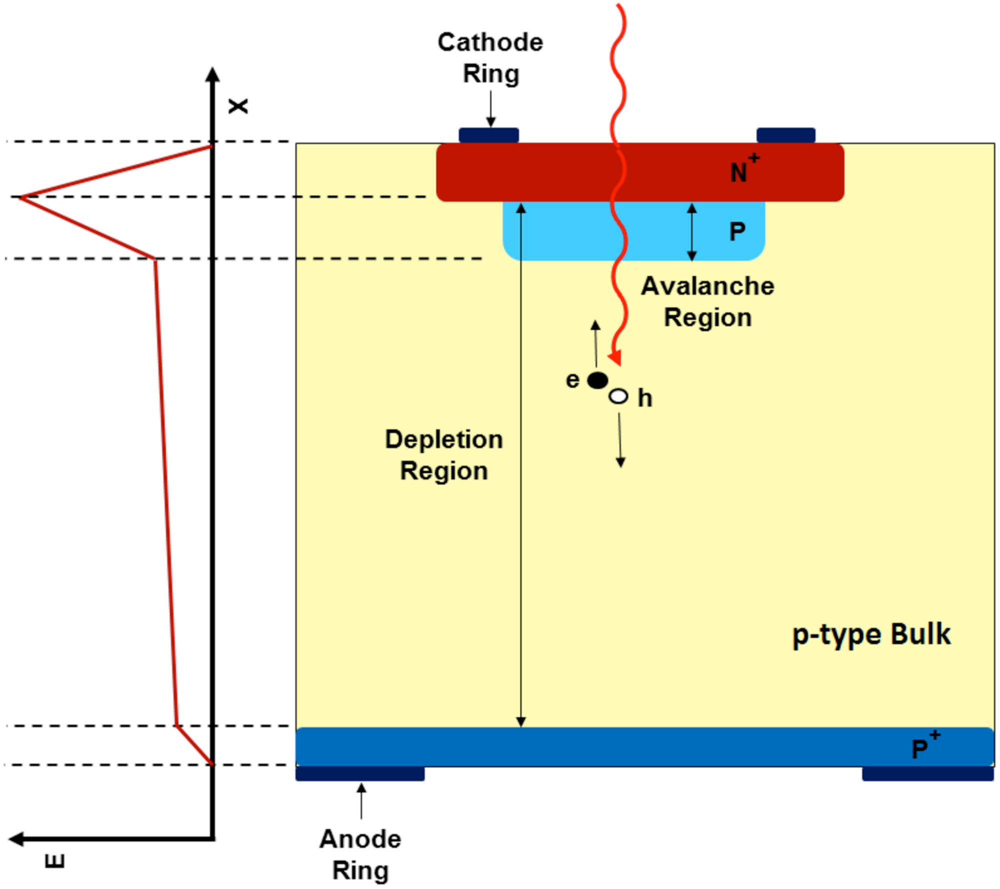
Middle Ring:
50% sensor overlap

Outer Ring:
20% sensor overlap



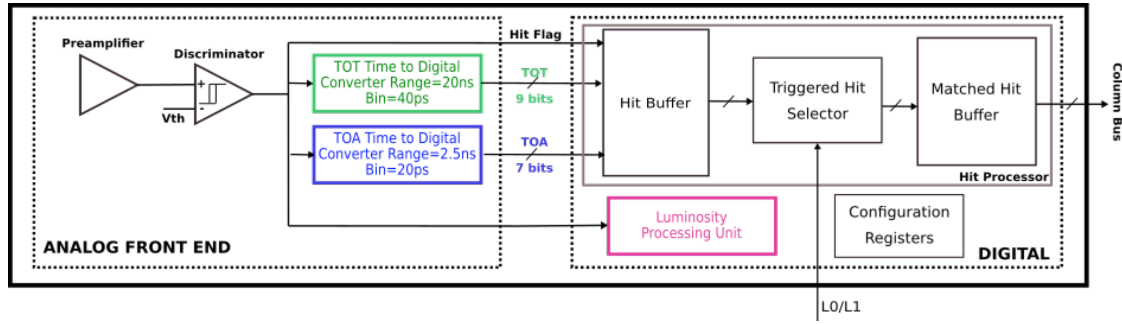
Low-Gain Avalanche Diodes (LGAD)

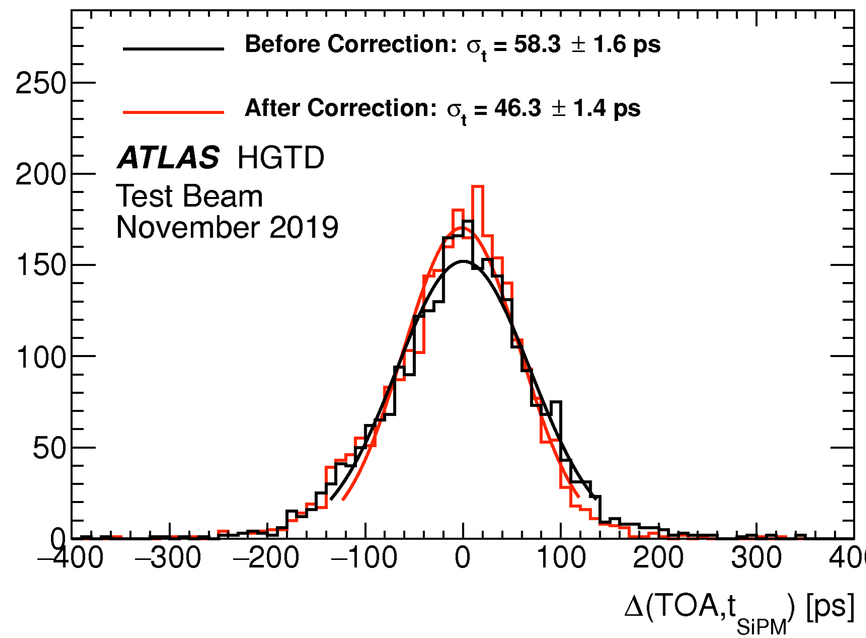
- Pad size of 1.3×1.3 , 5 µm thick
- Occupancy <10% at lowest HGTD radius (120 mm).
- Small dead areas between pads
- 15×15 pads, for 1.95×1.95 cm^2 total area



Front-end electronics: ALTIROC

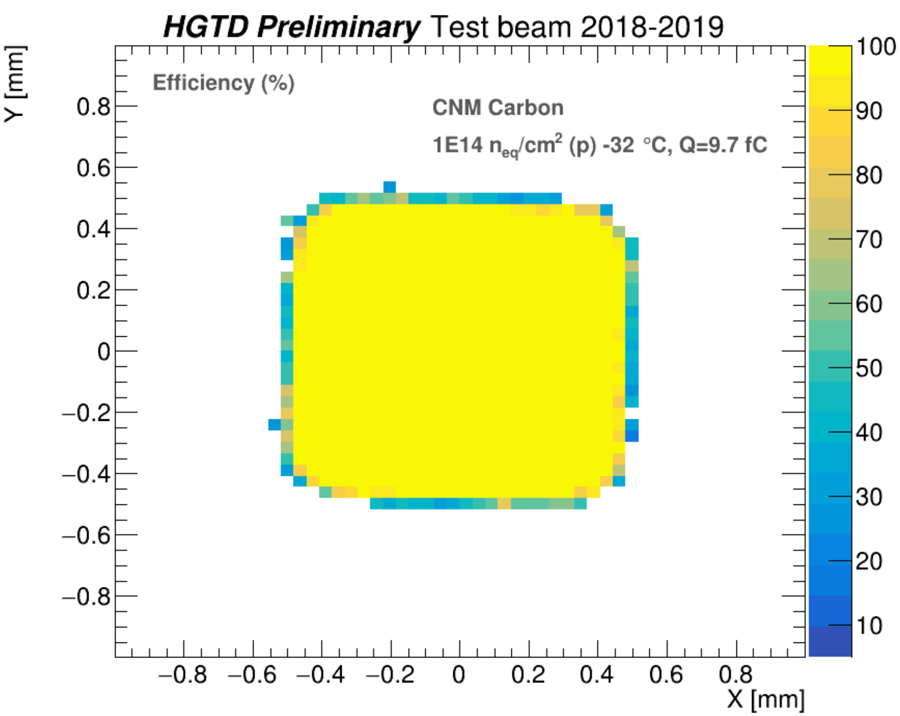
- Signal from each LGAD read out using the ATLAS LGAD Timing Readout Chip (ALTIROC)
- Bump-bonded to LGAD module
- 15x15 = 225 readout channels
- Channel= Analogue(Preampli fiers, Time Of Arrival TOA, Time Over Threshold TOT, CFD) + Digital data transmission
- Time resolution of 58 ps before corrections

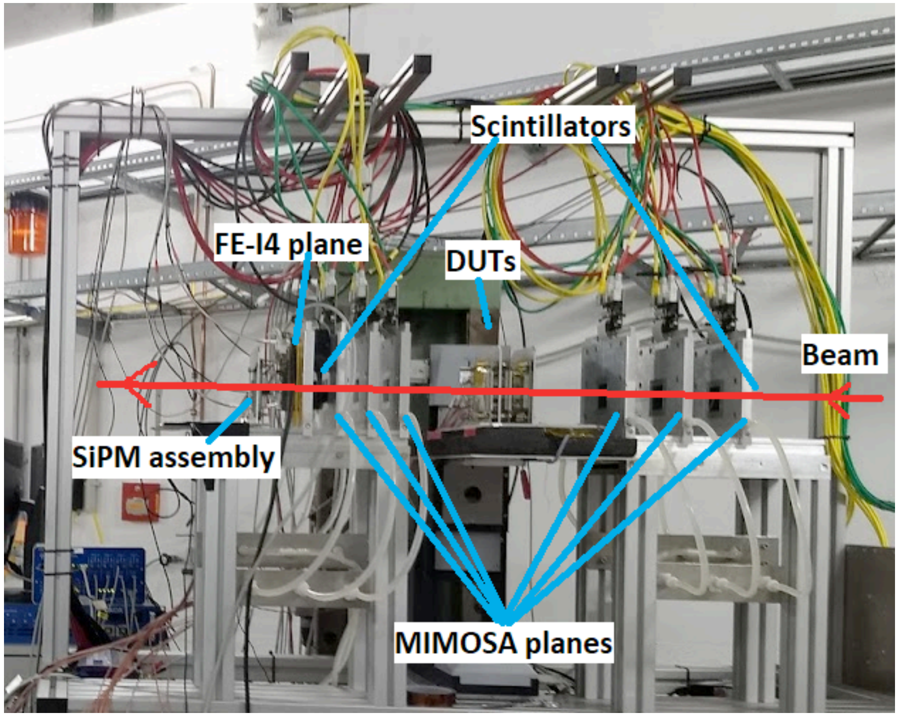




Test beam

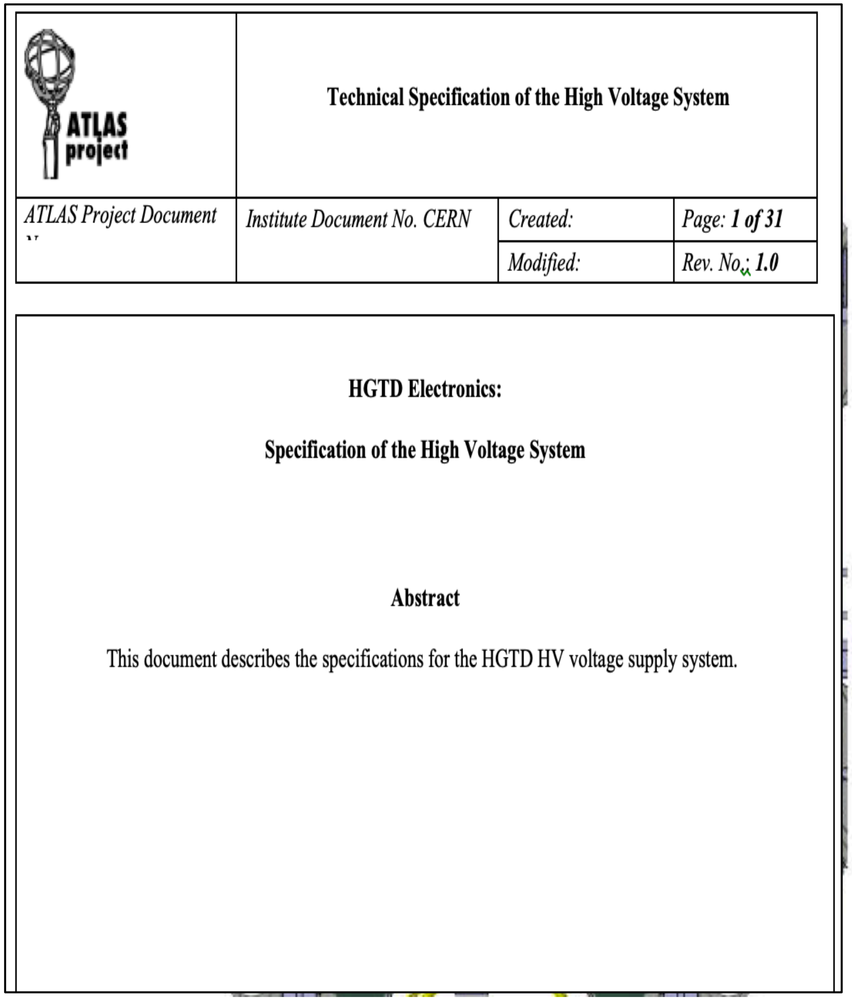
- Data collected in 2018-2019 with 120 GeV pion beam (CERN SPS) and 5 GeV electron beam (DESY).
- Hit efficiency defined as hits on sensor with > 2 fC
- Response is ≈100% in the active area





HGTD Involvement: HV Patch Panels

- Producing HV patch panels CERN group:
  - 16 patch panel boxes located around the calorimeter perimeter
  - Routing of High Voltage to HGTD detector
  - Filtering out AC noise
  - Preliminary layout done and prototype tested
  - Contributing to Specifications Review (SPR) document



ATLAS project	Technical Specification of the High Voltage System		
ATLAS Project Document	*Institute Document No. CERN*	*Created:*	*Page: **1 of 31***
		Modified:	*Rev. No.: **1.0***

HGTD Electronics:

Specification of the High Voltage System

Abstract

This document describes the specifications for the HGTD HV voltage supply system.

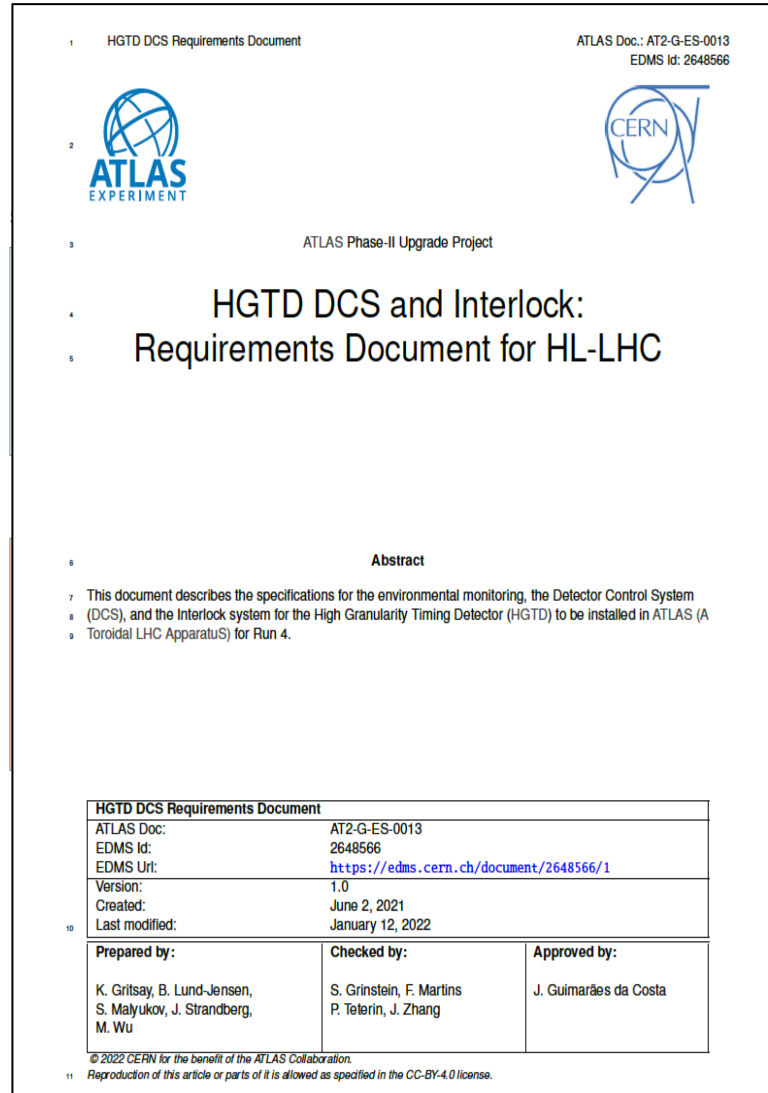


DCS and Interlocks

- HGTD DCS – ongoing work (Filipe):
  - Contributed to DCS Specifications Review document
  - Following SPR panel recommendations working on alternative for data transfer path separate from FELIX
  - Working on High Voltage DCS

- DCS and Interlocks – plans (Rui, Helena):
  - Plan to develop monitoring data transfer through FELIX or alternative solution – Rui
  - Plan to develop design for Interlocks – Helena
  - Helena's commitments imply a small re-scheduling



HGTD DCS Requirements Document

ATLAS Doc.: AT2-G-ES-0013
EDMS Id: 2648566

ATLAS Phase-II Upgrade Project

HGTD DCS and Interlock: Requirements Document for HL-LHC

Abstract

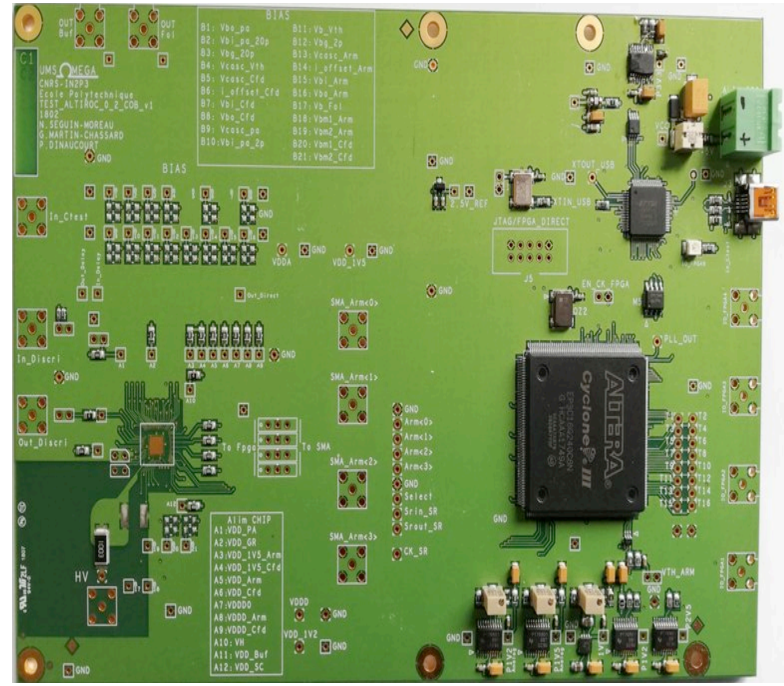
This document describes the specifications for the environmental monitoring, the Detector Control System (DCS), and the Interlock system for the High Granularity Timing Detector (HGTD) to be installed in ATLAS (A Toroidal LHC ApparatuS) for Run 4.

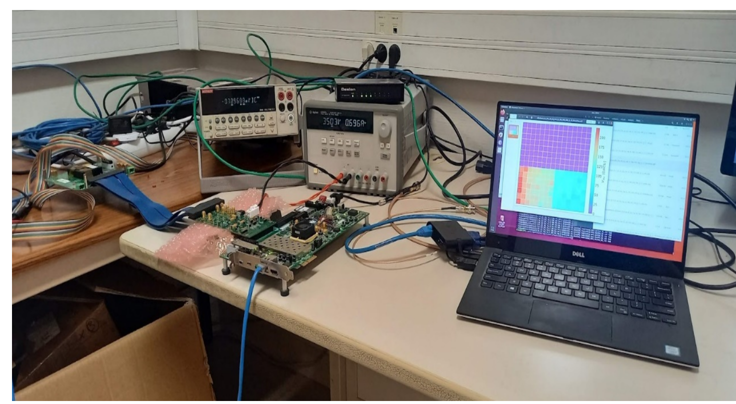
HGTD DCS Requirements Document	
ATLAS Doc:	AT2-G-ES-0013
EDMS Id:	2648566
EDMS Url:	https://edms.cern.ch/document/2648566/1
Version:	1.0
Created:	June 2, 2021
Last modified:	January 12, 2022

Prepared by:	Checked by:	Approved by:
K. Gritsay, B. Lund-Jensen, S. Malyukov, J. Strandberg, M. Wu	S. Grinstein, F. Martins P. Teterin, J. Zhang	J. Guimarães da Costa

Electronics: Altiroc

- Becoming involved in Altiroc testing:
  - In contact with Omega laboratory to install a test setup at LIP
  - Previous experience with Omega ASICs and frontend electronic design & production
  - Serious immediate problem in obtaining a Xilinx board (20 weeks delivery time… changed to 1 month)





Conclusions

- HGTD is expected to start data taking in 2028 and will be the first large-scale application of LGAD technology
- Will reduce pileup in the forward region and improve luminosity measurement
- LGADs and their readout ALTIROCs are optimised to reach a 30-50 ps per track up to the end of lifetime
- We are joining this project in several areas within our expertise

- References:

  – A High-Granularity Timing Detector for the ATLAS Phase-II upgrade, 30th Lepton-Photon, Jan 2022, Manchester, UK, ATL-HGTD-SLIDE-2021-745
  – **LHC**ATLAS Collaboration. Technical design report: A high-granularity timing detector for the ATLAS phase-II upgrade. Technical report, 2020. https://cds.cern.ch/record/2719855Reference